A Survey on Floorplan Representations in VLSI

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Abstract*—In the state of the art of computer designing interconnection of a huge number of circuit elements in a small enough area possess a challenge for the designers. This is possible if the task is divided into smaller independent modules. This is helpful for concurrent design of the individual modules as well. Interestingly the suitable placement and proper interconnection of these modules became an issue in this design. Right placement of the modules is an interesting study that needs to explore the computational aspects of geometrical shapes and appropriate graph theoretical representation. This is helpful for the automation of Floorplan and placement methods and useful in efficient realization of a huge circuit. Efficient representation of Floorplan is an interesting open problem and over few decades many researchers work on this problem to get optimal solution in terms of space and time. This work covers various representational approaches of Floorplan which should be beneficial for junior researchers, wants to start working on this area.*

***Keywords*—Floorplan,Sliceable Floorplan, Floorplan Representation, Non- sliceable Floorplan, Mosaic Floorplan, Binary tree, v-h tree, B* tree, O tree, Twin Binary tree.**

1. INTRODUCTION

In VLSI physical design after the Circuit Partitioning Phase the area of each circuit module, possible shape of each module, number of terminal in each module and their interconnection details (net list) are known which are used as the input to the next phase called Floorplan Phase. Floorplan refers to the relative positioning of the partitioned module. This is helpful to reduce the routing cost, signaling delay and design time. In integrated circuit optimal placement and positioning of block is an interesting open problem to the VLSI designers.For efficient Floorplan and Placement in VLSI design several factors are taken into observation such as shape of the Blocks using the aspect ratio of the blocks, routing decisions, Packaging Considerations. The aspect ratio of rectangle R defined as the ratio of its height h(R) and width w(R) i.e. h(R)/w(R).Shape flexibility of the soft rectangles (shape can be changed keeping the area constant) is said to be r if its aspect ratio resides in between 1/r to rand this soft rectangles makes the area optimized Floorplan and placement.In the operational mode circuit modules start generating heat so the circuit blocks that generate large amount of heat are kept as far as possible preserving the other Floorplanning constrain.

Floorplan Optimization problem defines the formation of suitable topology and sizing of flexible circuit modules [1]. A well-known approach for Floorplan topology generation is the graph dualization [2]. The inter module connectivity of the functional modules in Floorplan generally represented by an Adjacency Graph.A Floorplan and its adjacency graph have geometric duality relation. Rectangular Floorplan realisation of Adjacency Graph is called Rectangular Graph.Later area-optimal Floorplan generation based on graph dualization [3] and algorithms for the topology generation and area optimization [4] has been proposed for both sliceable and non-sliceableFloorplan. Area optimization algorithm for slicing Floorplan is polynomial time bounded whereas the area optimization problem for non-slicing Floorplan is NP –Hard [5].

2. TYPES OF FLOORPLAN

a. Sliceable and non-Sliceable Floorplan

A rectangular Floorplan obtained by making non-overlapping rectangular dissection by horizontal and vertical T-junctions likeline segments. Rectangular Floorplan is sliceable if it is obtained by recursively dividing a rectangle by horizontal and vertical cuts till the level of individual module otherwise called non-sliceable.

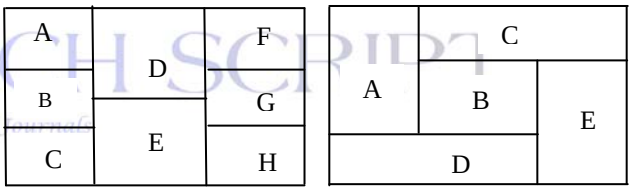

Fig. 1(a). Sliceable FloorplanFig. 1(b). non- Sliceable Floorplan

The number of Slicing Floorplan with n blocks where n>1 is equal to the twice the Schroder Number A_n[6] defined by:

$A_0=1; A_1=1;$

$A_n= (3(2n-3) A_{n-1}-(n-3) A_{n-2})/n;$

Two Floorplans are said to be equivalent if and only if their corresponding blocks have the same relative position i.e. one-to-one mapping between their modules and does not depends on the size of the modules.

b. Mosaic Floorplan

In Mosaic Floorplan [7] rectangular region divided into horizontal and vertical segments into rectangular region and each region corresponds to exactly one block and there be no empty space between modules.The number of distinct Mosaic Floorplans with n blocks is equal to the nth Baxter Number[8]

$$B(n) = (n+1C1)^{-1}(n+1C2)^{-1} \sum_{k=1}^{n}(n+1Ck-1)(n+1Ck)(n+1Ck+1)$$

Two Mosaic Floorplans are said to be equivalent if and only if both Floorplan generate identical Horizontal Constraint graph (a directed graph defines the horizontal relationship between the vertical line segments of a Floorplan) and Vertical Constraint graph (a directed graph defines the vertical relationship between the horizontal line segments of a Floorplan)

3. FLOORPLAN REPRESENTATION

Floorplan algorithms use analytical force-directed method because most of the Floorplanning problems are interactive in nature. Efficient Floorplan representation thus became an important issue as the performance criteria based on the geometrical representation of circuit blocks. Efficient Floorplan representation must satisfy two important characteristics, first, representation must be unambiguous i.e. unique Floorplan generated from the Floorplan representation and second, transformation between Floorplan representations to its corresponding Floorplan takes minimum time.Various kind of representation techniques are described below:

a. Binary tree

One of the earliest representations of the sliceable Floorplan is the Binary tree representation [9]. A sliceable Floorplan with n modules have in total (n-1) horizontal and vertical cut. Intersection of horizontal and vertical cut form T-cut junction. Binary Tree represents Floorplan with n circuit modules having2n-1 nodes with (n-1) internal node which are the operator (represents horizontal or vertical cut) and n external node(represents modules).

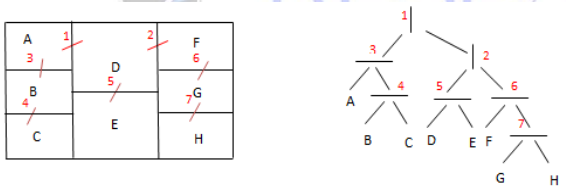

Fig. 2. Sliceable Floorplan and its equivalent Binary Tree.

Postorder traversal sequence of this tree is the compact representation of the Floorplan but during the reconstruction of Floorplan from that Postorder traversal sequence ambiguity arises which defines improper connectivity of functional modules.There is one to many relationships between Sliceable Floorplan and its equivalent Binary Tree. The upper bound on the number of possible binary tree representation for n modules Floorplan is given by the expression $O(n!2^{5n-3}/n^{1.5})$ [10].

b. V-h tree

The ambiguity problem of Binary tree representation eliminated in v-h tree representation.

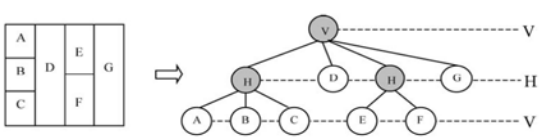

Fig. 3. Rectangular Sliceable Floorplan and its equivalent v-h tree representation.

V-h tree is a rooted ordered tree with each node represents a rectangle in the Floorplan. In this treeonly the leaf nodes represents the modules. There is one-to-one correspondence between v-h tree and its Slicing Floorplan [11].

c. Horizontal and Vertical Constraint Graph

The non-slicing Floorplan is more generalized and in practice arises more frequent than slicing Floorplan.

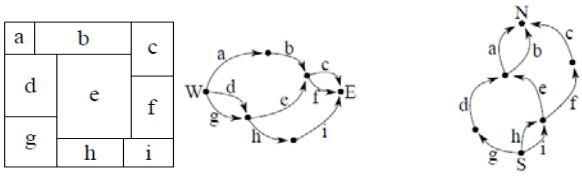

Fig.4. Mosaic Floorplan and its equivalent Horizontal and Vertical Constraint Graphs.

Non-slicing Floorplan cannot be represented using slicing tree. Horizontal constraint graph (HCG) and a vertical constraint graph (VCG) used to model a non-slicing Floorplan.

d. Bounded Slicing Grid (BSG)

S. Nakatake [12] proposed Bounded Slicing Grid (BSG) to represent non-sliceable Floorplan. A special *n*-by-*n* grid was devised for placing *n* blocks. This approach has n! $C(n^2,n)$ combinations and contains a lot of redundancy. The time complexity of the transformation is $O(n^2)$.Maggie and Wayne [13] proposeda new greedy algorithm based on the Bounded Slicing Grid structure, which runs in linear time and based on this structure, they proposed SIA-based local search and GA-based global crossover to L-shaped, T-shaped blocks and obtain high density packing of rectilinear blocks.

e. Sequence Pair (SP)

Sequence pair (SP) is an ordered pair of module name sequences used for the representationof General Floorplan [14].For each module i, two rectilinear curves right-up locus and left-down locus are need to be drawn and the union of this two loci of module i forms the positive locus of module i. Negative loci can be obtained similar to the positive loci. The difference is that a negative locus is the union of the up-left locus and down-right locus. Positive locus and negative locus form the sequence pair. By

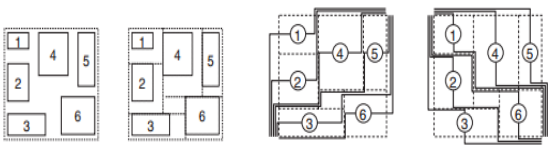

Fig. 5 Floorplan and its positive loci and negative loci make the sequence pair (124536, 326145).

Searching this space using simulated annealing, large numbers of modules have been packed efficiently [15] applied on MCNC benchmark *ami49* with a conventional wiring area estimation method, and obtain a highly promising placement.

f. Simulated Annealing(SA)

Simulated Annealing (SA) probably the most popular method for Floorplanoptimization [16].Using appropriate data structure, a feasible adjacent Floorplan can be obtained in $O(n^2)$ time[17] and the reachability from any Floorplan to any other in the proposed solution space will be proved.Later Simulated Spheroidizing Annealing Algorithm (SSAA) has been developed based on a Simulated Annealing Algorithm (SAA)[18]. The proposed SSAA algorithm is also found more efficient for problems of larger sizes.

g. B tree*

B* tree is an ordered tree and efficient data structure to represent compact non-sliceable Floorplan. In a compact Floorplan, no modules can move towards left or bottom in the Floorplan [19]. This approach was widely approved by the researchers as in this tree Search, Insertion can be done in constant time and Deletion in linear time.

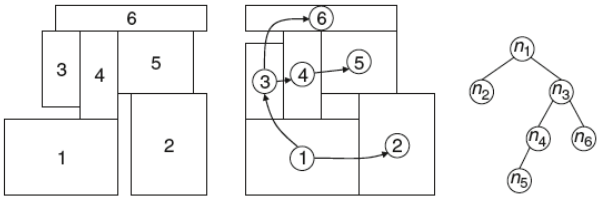

Fig. 6.Floorplan and its B* tree representation

The Experimental results on MCNC benchmarks show that the B*-tree representation runs faster than other representation and consumes less memory. Hybrid algorithm based on B* tree representation improve the area utilization [20]. Hybrid Evaluation Algorithm for VLSI Floorplanning based on B* tree was proposed later [21]. This algorithm also applied on multilevel Floorplanning Framework and its output is effective and efficient.

h. Corner Block List(CBL)

Corner Block List is another efficient topology representation for non-slicing Floorplan [22]. Parallel algorithm for non-Slicing Floorplan using CBL was proposed later [23]applied on MCNC benchmarks. Experimental results that came out is quite good on the basis of operating speed.

i. Transitive Closure Graph(TCG)

Transitive Closure Graphcombines the advantages of Sequence Pair, Boundary Sequence Grid and B* tree [24] applicable for non-Slicing and other Floorplan having the solution space O (n!) ^{2} with the packing time$O(n^2)$.

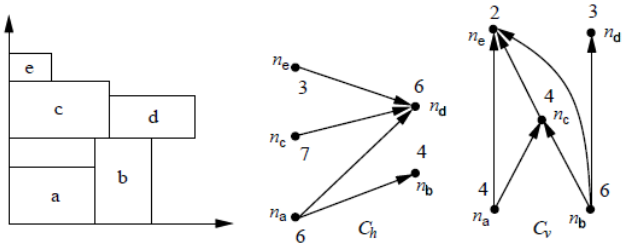

Fig. 7. Floorplan and its Transitive Closure Graph representation.

Later combining the advantages of Sequence Pair and Transitive Closure Graph new representation has been proposed TCG-S[25]which is stronger representation than TCG and provides better placement.

j. Ordered Tree(O-tree)

An O-tree represents partial topological information, which together with the dimensions of all blocks describes an exact Floorplan [26].

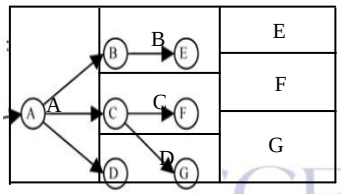

Fig.8.Floorplan and its Ordered tree representation.

The O-tree has a combination number $O(n!2^{2n-2}/n^{1.5})$. This approach produces a Floorplan in linear time.

k. Twin Binary Tree

Twin Binary tree is the most efficient representation for Mosaic Floorplan [27].

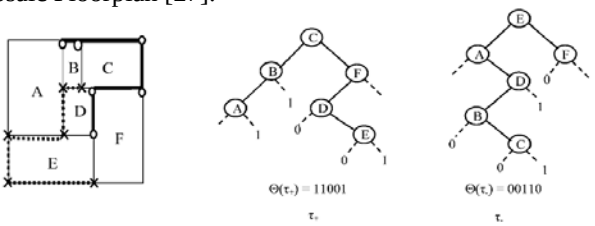

Fig. 9. Mosaic Floorplan and its Twin Binary tree representation.

For every Mosaic Floorplan two Binary trees are constructed and from that trees two binary strings are formed which reconstruct the Floorplan uniquely. This representation has the solution space$O(n!2^{3n}/n^{1.5})$and the packing time O(n).

4. CONCLUSION

This paper describes various representation techniques of sliceable, non-Sliceable and mosaic Floorplans. Advantages and disadvantages of various representations (based on search space, complexity of representation and

reconstruction etc.) can be figure out from this work. It's helpful for new and working researchers to understand the present scenario and to develop better solution in future.

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