Multilevel Inverter Based Dstatcom For Compensation of Reactive Power and Harmonics

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Abstract— *A five-Level Cascaded H - bridge (CHB) Inverter as Distribution Static Compensator (DSTATCOM) is used in Power System (PS) for compensation of reactive power and harmonics. The DST ATCOM helps to improve the power factor and eliminate the Total Harmonics Distortion (THD) drawn from a Non-Liner Diode Rectifier Load (NLDRL). The D-Q reference frame theory is used to generate the reference compensating currents for DSTATCOM while Proportional and Integral (PI) control is used for capacitor dc voltage regulation. A CHB Inverter is considered for shunt compensation of a 11 kV distribution system. Finally a level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) techniques are adopted to investigate the performance of CHB Inverter.*

Keywords— DSTATCOM; Level shifted Pulse width modulation (LSPWM); Phase shifted Pulse width modulation (PSPWM); Proportional-Integral (PI) control; CRB multilevel inverter; D-Q reference frame theory

1.INTRODUCTION

Voltage sags are one of the most dominating power quality assets, which dragged the attention of many researchers as the sensitivity of loads are increasing due extensive usage of power electronic devices. Fault at distribution level, sudden increase of loads, motor starting are some of the causes of the voltage sags. Such sudden variations of voltage are undesirable for sensitive loads. These undesirable voltage sags can be mitigated by connecting controlled devices either in series or shunt to the load. A few of such devices are dynamic voltage restorer (DVR) and DSTATCOM (Distribution Static Compensator). Both these devices require voltage source converters to satisfactory operation. Many topologies have been proposed in recent past for voltage source converters. Multilevel inverter has drawn attention of many researchers. There are three topologies of multilevel inverters-cascaded, flying capacitor and diode clamped, each having its own advantages in various applications. Cascaded H-Bridge multilevel inverter is one of the popular converter topologies used in high-power-medium-voltage (MV) drives. H-Bridge cascaded inverter is one of the popularly used converter topology. The H Bridge cells are normally connected in cascade on their ac side to achieve medium-voltage operation and low harmonics distortion. The CHB inverter using v multilevel topology offers the following advantages.

- Its structure will be simple and requires fewer components
- Simplicity of structure so the packaging layout is much easier.
- To reaches high voltage and reduce harmonics by their own structure.
- Generates multistep staircase voltage waveform similar to pure sinusoidal output voltage by increasing the number of levels.

The Multilevel inverters require advanced PWM strategies like level shift, phase-shift or phase deposition. Among these PWM strategies phase-shifted PWM.

2. SHUNT VOLTAGE CONTROLLE [DISTRIBUTION STATIC COMPENSATOR (DSTATCOM)]

The principle of shunt voltage controller is fig1. The actual controller has the same configuration as the series controller. But instead of injecting the voltage difference between the load and the system, a current is injected which pushes up the voltage at the load terminals. The load voltage during the sag is the superposition of voltage due to the system and the voltage change due to controller. A DSTATCOM does not contain any active power storage and thus only injects or draws reactive power. Limited voltage sag mitigation is possible with the injection of reactive power, but active power is needed if both magnitude and phase angle of the pre-event voltage needs to be kept constant. A DSTATCOM consist of a five-level voltage source converter (VSC), an isolated dc energy sources and coupling transformer connected in shunt to the distribution network. The dc voltage across the storage device in to a set of three-phase ac output voltage by using VSC converters. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. A multifunction topology which can be drawn from VSC connected in shunt with the ac system.

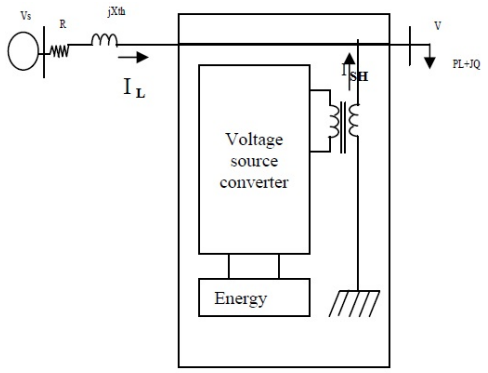

Fig.1. Schematic diagram of DSTATCOM

The multifunction topology can be achieved from VSC connected in shunt with the ac system which can be used for up to three quite distinct purposes.

- Power factor correction
- Current harmonics elimination
- Voltage regulation and compensate of reactive Power.

Fig.1 the shunt injected current Ish corrects the voltage sag by adjusting the voltage drop across the system impedance Zth. The value of Ish can be controlled by adjusting the output voltage of the converter. In DSTATCOM the voltage sag correction depends on the value of Z_{th} (or) fault level of the load bus. The desired voltage correction can be achieved without injected any active power in to the system. When I_{sh} minimized, the same voltage correction can be achieved with minimum apparent power injection in to the system.

3. CONTROLLER

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load is connected, under system disturbances. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the Fundamental Frequency Switching (FFS) methods favored in FACTS applications. Besides, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses. The controller input is an error signal obtained from the reference voltage and the value rms of the terminal voltage measured. Such error is processed by a PI controller the output is the angle δ, which is provided to the PWM signal generator. It is important to note that in this case, indirectly controlled converter, there is active and reactive power exchange with the network simultaneously: an error signal is obtained by comparing the reference voltage with the rms voltage measured at the load point. The PI controller process the error signal generates the required angle to drive the error to zero, i.e., the load rms voltage is brought back to the reference voltage.

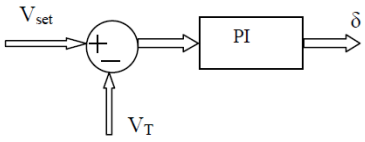

Fig.2.PI Controller of DSTATCOM

4. MODULATION STRATEGY

Usually stair case modulation is commonly used for cascaded H-bridge converters. For SCM, the switching instants of each module are calculated offline to attenuate certain harmonics .In that case dc link voltage has to be varied in accordance to the desired ac output voltage. Due to bulk dc link voltage dynamic response slows down. As the voltage sag duration ranges from half cycle to 30 cycles, fast dynamic response is required for the DVR application. Based on this consideration, Phase shifted PWM modulation scheme is adopted to maintain a relatively constant dc link voltage while achieving the fast dynamic response required of the output voltage by varying modulation index .Multilevel inverters require carrier based modulation schemes due to higher levels. The carrier-based modulation schemes for multilevel inverters are classified as phase shifted and level-shifted modulations. Multilevel inverter with m voltage levels requires (m-1) triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the peak-peak amplitude with phase shift between any two adjacent carrier waves given by

$$\emptyset = \frac{360}{m-1}$$

The modulating angle is applied to the PWM generators in phase A. The angles for phases B and C are shifted by 240^0 and 120^0, respectively. It can be seen in that the control implementation is kept very simple by using only voltage measurements as the feedback variable in the control scheme. The speed of response and robustness of the control scheme are clearly shown in the simulation results.

A. Cascaded H-Bridge Multilevel Inverter

The number of output voltage levels of CHB is given by 2n+l and voltage step of each level is given by Vdc/2n, where n is number of R-bridges connected in cascaded. The switching mechanism for 5-level CHB inverter is shown in table-1.

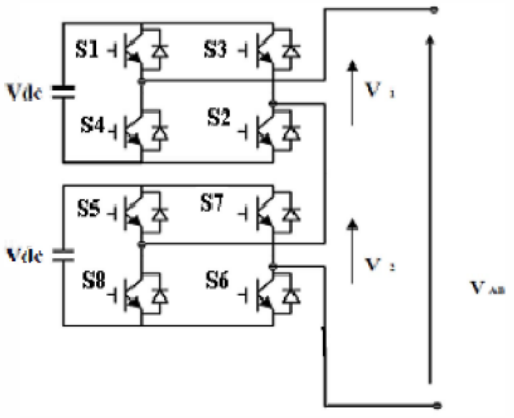

Fig.3. Circuit Diagram of 5-level CHB Inverter model

TABLE I. SWITCHING TABLE FOR 5-LEVEL CHB INVERTER

Switches Turn ON	Voltage Level
S1,S2	Vdc
S1,S2,S5,S6	2Vdc

S4,D2,S8,D6	0
S3,S4	-Vdc
S3,S4,S7,S8	-2Vdc

B.PWM Techniques for CHB Inverter

1.Phase Shifted Carrier PWM (PSCPWM)

Fig-4 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distri bution among the cells. A carrier phase shift of 1800 /m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multi level output waveform with lower distortion.

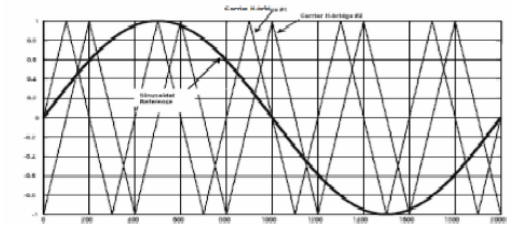

Fig.4. Phase Shifted Carrier PWM

2.Level Shifted Carrier PWM(LSCPWM)

Fig-5 shows the Level shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar width modulation and bipolar pulse pulse width modulation respectively, providing an even power distri bution among the cells. A carrier Level shift by 1/m (No. of levels) for cascaded inverter 1S introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

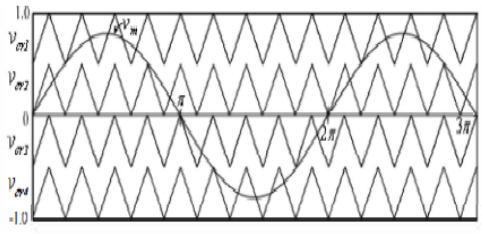

Fig.5.Level Shifted Carrier PWM

5.MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Fig.6.shows the Matab/Simulink power circuit model of DSTATCOM. It consists of five blocks named as source block, non linear load block, control block, APF block and measurements block. The system parameters for simulation study are source voltage of 11 kv, 50 Hz AC supply, DC bus capacitance $1550e^{-6}$ F, Inverter series inductance 10 mH, Source resistance of 0.1 ohm and inductance of 0.9 mH ,Load resistance and inductance are chosen as 30mH and 60 ohms respectively.

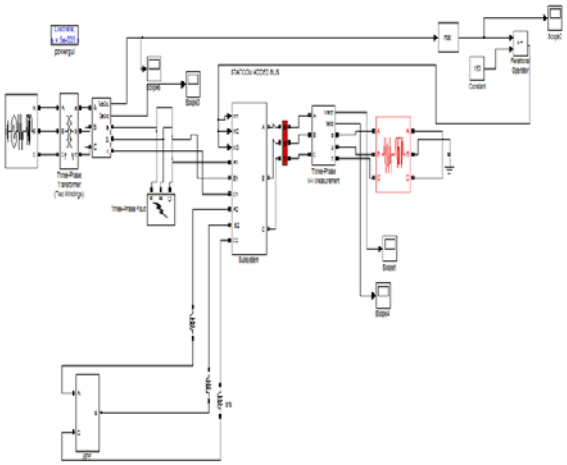

Fig.6.MATLAB/Simulink Power Circuit Model

Fig.7. shows the phase voltages of five level output of phase shifted carrier PWM inverter.

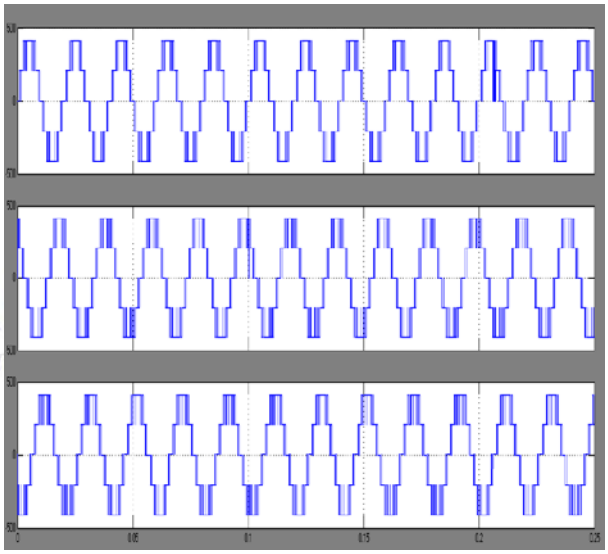

Fig .7.Five level PSCPWM output

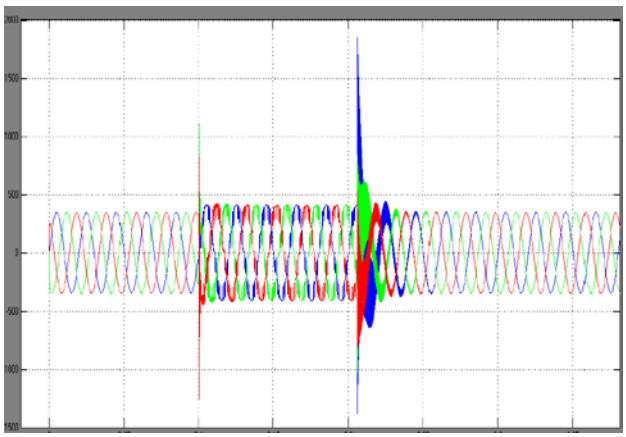

Fig.8. Load Voltage

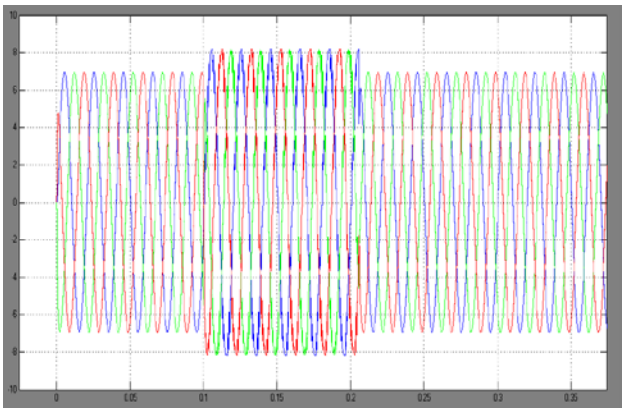

Fig.9. Load Current

The three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOM even though load current is non sinusoidal source currents are sinusoidal. The THD of source current without DST ACOM is 7.49%, while that of load current is 3.76%.

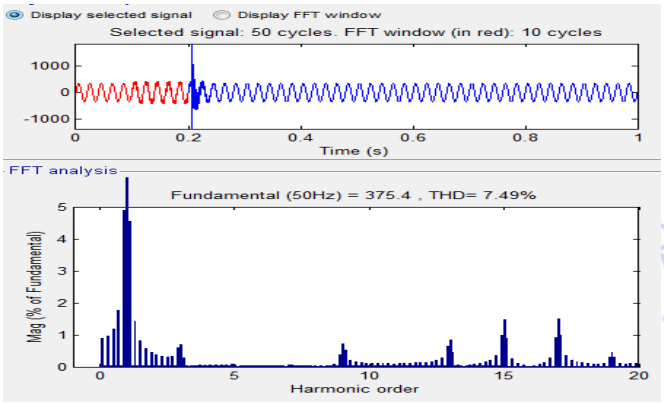

Fig.10. Harmonic spectrum of Load Voltage

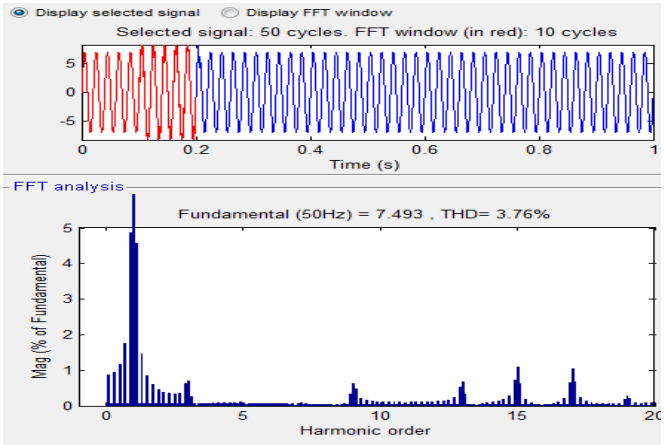

Fig.11. Harmonic spectrum of load current

6.CONCLUSION

The cascaded 5 level inverter topology has been presented for shunt active power filter (DSTATCOM). The advanced pulse width modulation technique (PSPWM) is used for 5 level inverter. The Cascaded H-bridge multilevel topology is shown as one of the more suitable topologies for reactive power compensation applications. The evolution on the power semiconductor technologies has allowed the increase of switching frequencies and the use of PWM modulation techniques.The advantages of cascaded inverter in modeling of DSTATCOM are presented clearly. The following observations are made based on simulation results.

• With cascaded multilevel inverter dc voltage requirement can be reduced, i.e with low dc voltage higher ac voltages can be produced.

• As dc voltage requirement is less, the proposed topology is more economical.

• Filter at the output of the inverter can be eliminated with multilevel topology further reducing the cost of the filter.

• The total harmonic distortion is well within the acceptable limits

A DSTATCOM with five level CHB inverter is investigated. Mathematical model for single H-Bridge inverter is developed which can be extended to multi H Bridge. The source voltage , load voltage , source current, load current, power factor simulation results under nonlinear loads are presented. Finally Matlab/Simulink based model is developed and simulation results are presented.

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