DYNAMIC OVERDRIVING CURRENT MODE SIGNALING FOR ON-CHIP INTERCONNECTS TO REDUCE POWER DELAY AND AREA

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Abstract*—An efficient scheme for low power high-speed communication over long on chip interconnects is Current-mode signaling (CMS) with dynamic overdriving technique. The Existing Scheme of Driver Pre-emphasis technique using Current Mode Signaling scheme with Feedback is implemented. CMS-Fb improves speed and reduces dynamic power consumption. Although it consumes static power, there exists a direct tradeoff between delay and static power. The proposed CMS scheme is fabricated in 180-nm CMOS technology. The CMS - smart bias scheme eliminate the Feedback and employs the corner aware bias and ring oscillator as delay element. CMS-Smart bias reduces the power consumption but increases the delay. CMS-Active bias scheme further reduces the area , power and delay by replacing the delay element and Bias circuit. Dynamic over-driving with CMS – Active bias is adopted for variation analysis which improves the area, power, delay, energy and EDP value over voltage mode signaling scheme. Delay measurement Scheme is an eminent application designed to prove the efficiency of CMS -Active bias circuit using dynamic overdriving technique.*

Keywords*— Current Mode Signaling, Dynamic overdriving, Active bias, On-chip Global Interconnects, D-latch, Buffer and Voltage Divider.

1. INTRODUCTION

In VLSI Technology, continuous scaling of the device improves the performance of the circuit. Interconnects are the dominating factors for reducing power consumption in Integrated circuits. The impact of supply voltage reduction in performance on current mode circuits is low compared with Voltage mode circuit. The usefulness of Current mode circuits is combating the difficulties arising from the reduction of the supply voltage which results in the increase of speed. Compared with the voltage mode signaling , Current mode signaling is faster(three times). Our proposed CMS-Active bias is implemented in 180nm technology. Dynamic overdriving current mode signaling scheme performs the variation analysis. It decreases the the delay on the interconnect.CMS scheme is based on the low voltage swing and reduces the noise margin[12]. Voltage swing is reduced by Dynamic overdriving scheme .CMS Scheme reduces the delay and improves the power related to the previous schemes. CMS-Smart bias does not rely on the mismatching of the transistor parameters. Current mode signaling (CMS) is a promising solution since it has the potential to reduce both the dynamic power and delay [16] .CMS scheme consumes static power and exhibits a direct tradeoff between speed and power consumption [12].It is based on reduction in voltage swing and decreases the noise margin of data communication system. It consumes much less power compared to improved repeater circuits (such as self-timed repeater[4],boosters[7] and signaling scheme such as near speed of light[18] and transition aware global signaling[2].Dynamic overdriving CMS scheme results improvement in delay, energy and EDP over voltage mode signaling scheme[13].Current mode transmission offers the possibility for improving latency, throughput and power. The main advantage of CMS scheme is the reduction in noise margin.[14].

CMS-Fb SCHEME WITH DRIVER PRE –EMPHASIS

Driver pre-emphasis is a technique of supplying large current or voltage to the line during transition of the input and very small current or voltage in the steady state. In CMS-Fb, the transmitter has a strong driver and a weak driver. The strong driver supplies a large current to the line during transition to the transistor and the weak driver provides a small steady state current to the line. NAND and NOR gates turn on the strong driver for a short duration, which is controlled by a feedback inverter. At the transmitter end, the strong driver is turned off after the line voltage crosses the switching threshold of the feedback inverter. At the receiving end, the line voltage is held near VMRx, which employs a feedback and makes the line voltage swing around V MRx , that is the switching threshold of inverter amplifier. The product of the static current and small signal input impedance gives the steady state voltage swing of the line. The output is measured at the end if the inverter amplifier.VMTx and V Mrx are considered to be the the transmitter and receiver which are placed far apart .Consider V MTx is less than V MRx . Receiver holds the line voltage at V MRX, which is greater than V mrx . As a result, the strong driver is turned on to pull the line voltage below V MTx. When the line voltage is pulled below V MTx , the strong diver is turned off. When the line voltage rises to V MRX ,the strong driver is activated. Even if the input is at the constant logic “0” ,the line voltage swings between V MTX and V MRx .While

"0" to "1" transition in the input the strong driver is turned off before receiver voltage has crossed V MRx

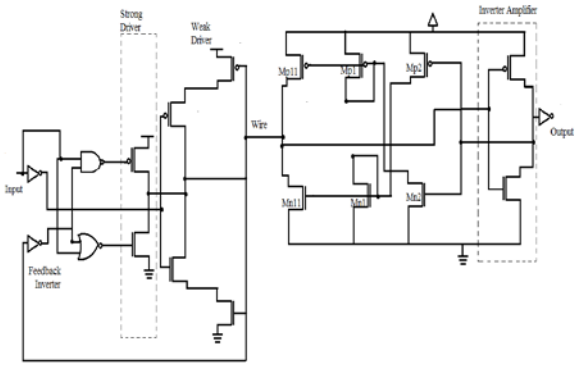


Fig 1. CMS-Fb with drive pre-emphasis

While "1" to "0" transition ,even after the transmitter's line voltage crossed V MRX the strong driver remains active. As a result , the delay for "0"to "1" transition is more compared to "1"to "0" transition. Likewise ,if V MTx > V MRX ,the fluctuations in line voltage occurs even if the line voltage is kept at logic "1" and "1" to "0 " tractions is slower than "0" to "1".Significant reduction in the throughput occurs ,even though, "0" to "1" and "1" to "0" transition differ by a large amount.

2. CMS-SMART BIAS SCHEME

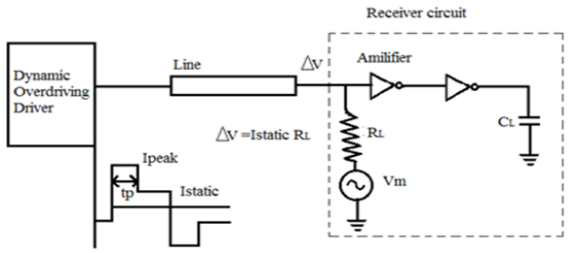
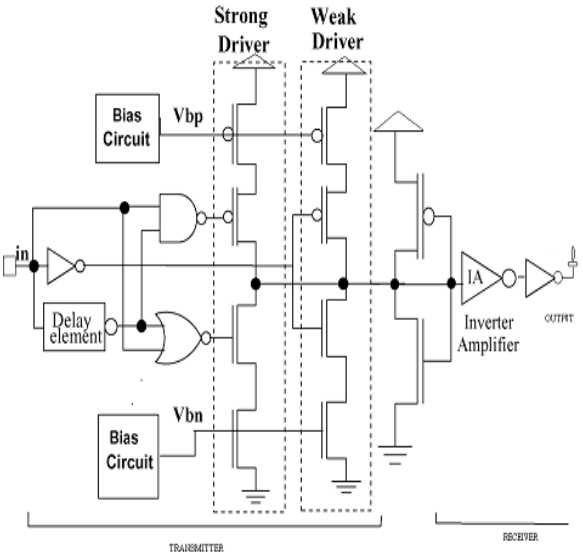


Fig 2. Model of dynamic overdriving CMS scheme

Dynamic overdriving CMS Scheme provides improvement in delay, Energy and EDP over voltage mode signaling scheme. The model of dynamic overdriving CMS Scheme is established to provide the effects of various design parameters based on the signaling schemes. It consists of driver and receiver circuit. The driver circuit acts as a current source and receiver circuit acts as a terminator circuit followed by an inverting amplifier. During transition the delay supplies large current to the line. The Voltage swing on the line is given by ΔV= I static * R L .The rise and fall delay of the link should be equal. During low to high and high to low transition the peak current supplied by the driver must be equal.

A. Transmitter and Receiver Circuit

The proposed CMS Smart bias scheme contains transmitter and receiver. The proposed transmitter employs two drivers, a strong and weak driver with NAND and NOR gates, where the operation is similar to CMS –Fb scheme. To control the time duration of the strong driver (feedback is used in CMS-Fb), the delay element is used in CMS-Smart bias. The proposed receiver comprise of the diode connected PMOS and NMOS (Terminator Inverter) followed by inverter chain. Terminator inverter holds the line voltage near Vmrx (switching threshold). Inverter amplifier along with the subsequent inverters converts the small line voltage swing to digital logic level.



In CMS –Smart bias ,the proposed bias element is Corner aware bias circuit and the proposed delay element is ring oscillator. The performance of the proposed circuit does not depend on the transistor matching condition since the transmitter and receiver circuit does not have any local feedback connections. The throughput increases as the rise delay and fall delay are equal. In CMS-Fb ,the feedback increases the delay and the power consumption is reduced. In CMS-Smart bias, power increases and the delay is reduced. The Corner aware bias circuit is obtained from the resistance based circuit in which the long channel MOS will act as a resistance because of the threshold voltage and gain. Hence, the long channel transistor acts as load and Short channel can act as sensor device.In this circuit there is a trade-off between area of a resistor and power consumption. This corner aware bias is dependant on the process characteristics. In order to minimize process dependence, a bias circuit should sense the process corner and adjust the bias to compensate for the variation. But in CMS-Active bias, power and the delay are reduced.CMS-Active bias is independent of the temperature and provides more stability.

B. Bias Generation Circuit

Voltage Divider Bias

A Voltage divider network consists of resistors R1 and R2,acts as a potential divider, where the voltage is divided among the series of the resistors. In the voltage divider bias,the voltage is applied at the one end of the series and other end is grounded ,the voltage among the resistors would be a fraction of the input voltage and dependant on the ratio of the resistance. The output voltage is a fraction

of the input voltage. The operating point of the transistor can be made independent of β by proper selection of resistors R1 and R2.The most important stabilization component in the voltage divider bias circuit is emitter resistance RE, which tends to make the operating point independent of the parameter change. The changes in the bias value of IC automatically changes the input voltage, which have opposite effect on IC, tend to restore IC to its original value. The use of the emitter resistor is to stabilize the bias point and is called emitter stabilization. Voltage divider bias circuit is also called potential divider bias, emitter bias or self bias. Despite the fluctuations in the ß,it maintains the stability of the current gain.

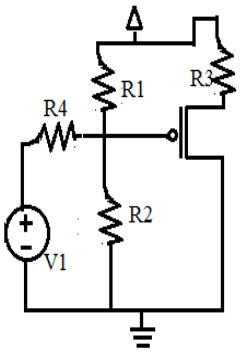


Fig 4. Voltage divider Bias

Drain Feedback Bias

Drain feedback circuit has a feedback across gate terminal and the drain terminal through a resistor. The Drain feedback bias configuration employs negative feedback to prevent thermal run away and stabilize the operating point , so any thermal runaway will induce a voltage drop across the RC resistor that will control the transistor base current. The drain voltage Vdd is fed back to the gate terminal through feedback resistor ,which does not carry any current. Hence drain voltage is equal to the gate voltage. Feedback resistor provides a very stable Q-point by reducing the effect of variations in current gain(β).As β increases with temperature, which results the increase in collector current Ic and in turn produces more voltage drop across RL, lowering the collector voltage, and IB is reduced. Hence the circuit tends to maintain a stable value of collector current keeping the Q-point fixed. Drain feedback bias is also called as collector feedback bias.

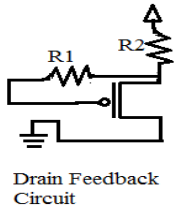


Fig 5. Drain Feedback Bias

Current Mirror

Current mirror is used to reflect the input reference current through active devices keeping the output current constant. Ideally ,the output current is equal to the input reference current multiplied by a desired current gain. If the gain is unity, the input reference current is replicated to the output, hence, it is known as the current mirror. In practice, the output current is not an accurate reflection of the input reference current, since the real transistor level of the current mirror suffer many variations from ideal behavior.

C. Delay Elements

Ring Oscillator

Ring oscillator is a combination of delay stages in cascade, which is connected in closed loop .The attractive features of ring oscillator are simple in design, oscillations is achieved at low voltage and provide wide tuning range. The oscillation frequency depends on the propagation delay and the number of the stages. To attain self sustained oscillation, the ring must provide a phase shift of 2π and the unity gain voltage. Each delay stage must provide a phase shift of π=N, where N is the number of delay stages.

D-Latch

When the clock input is high ,the D latch is used to capture or 'latch' the logic level present on the Data line. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the D input is trapped in the latch. Compared to other delay schemes ,the power consumption and delay is reduced. Latches are used as temporary buffer. When they are enabled, the output changes immediately when their inputs change.

Buffer

The stages of gate will result in buffer function where the output logical state is same as the input logical state. In a logic gate, the number of edges in the transients at the output of the gate may equal to the number of arriving signals at the gate.. This device is capable of transforming input signals into sharply defined, jitter-free output signals. This device ensures very low static and dynamic power consumption.

3. CURRENT MODE SIGNALING SCHEME USING ACTIVE BIAS CIRCUIT

CMS scheme with active bias is related to the CMS scheme with smart bias. The transmitter end is similar to the CMS smart bias, to control voltage swing. The Bias element acts as a current source, in order to provide the bias voltage to the strong and weak driver. The delay element controls the duration of the strong driver. The receiver end consists of the inverting amplifier and the inverter in order to reduce the mismatch condition. Implementation of the CMS-active bias using voltage divider and drain feedback circuits is proposed .Voltage divider bias element can be used to scale down the very high input voltage and adjust the level of the signal, since it divides the voltage across the resistor network and in D latch, when the state of the data line changes , the output follows the input. which results in

the reduction of power ,delay and area. The drain feedback consists of the feedback resistor, which stabilizes the operating point. The major drawback in current mirror is the output transistor which creates fluctuation and contributes to the noise. It exhibits a tradeoff between power and delay.

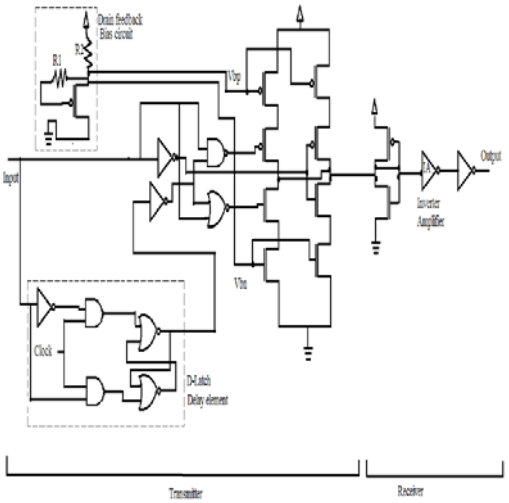


Fig 6. CMS Scheme-Active Bias with Drain Feedback and D Latch

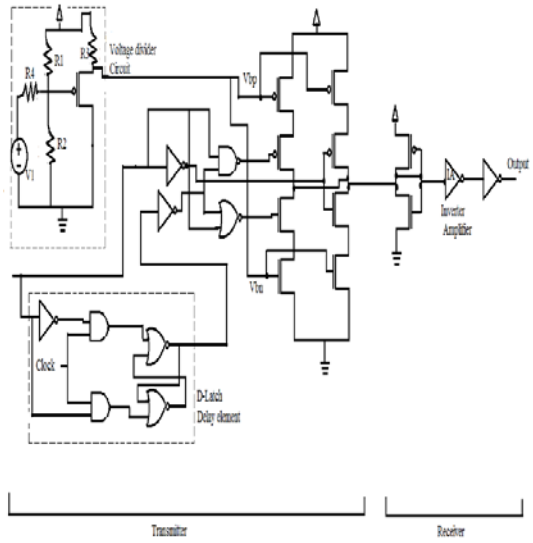
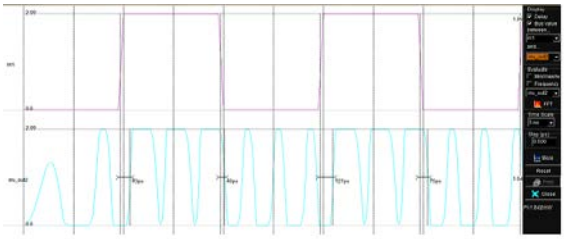


Fig 7. CMS Scheme – Active Bias with Voltage divider and D Latch

4. PERFORMANCE AND COMPARISON OF VARIOUS CMS SCHEME SIMULATION AND RESULTS

The parametric analysis of various Current Mode signaling scheme and the waveforms are estimated. Two types of the bias circuit are used in CMS scheme to reduce power, delay and area and also to improve the signal transmission speed over on–chip interconnects. The bias circuits are drain feedback and voltage divider. The above circuits are implemented in 180 nm technology. In CMS-Smart bias scheme ,static power consumption is less compared to CMS-Fb. When the rise delay and fall delay are equal, the throughput increases. Consequently, the system performance increases.



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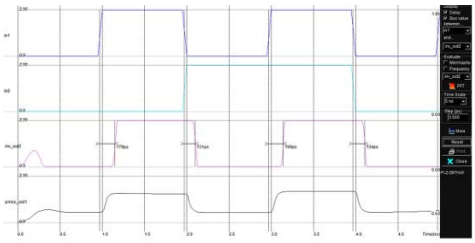

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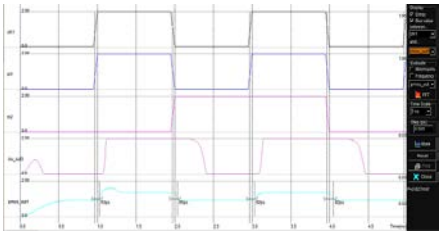

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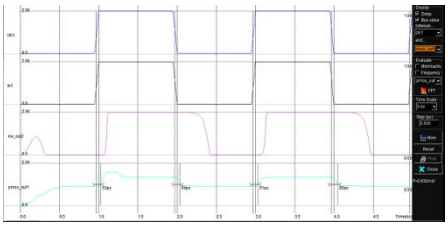

(d)

Fig 8. Analysis of Waveform of a)CMS-Fb b)CMS-Smart bias c)CMS-Active bias with Drain feedback d)CMS-Active bias with Voltage divider

The table 1 shows the estimation of the performance characteristics of the CMS –Active bias circuit and tabulated. we summarize that the circuit with D-Latch is more efficient than the other delay elements. As compared with ring oscillator and buffer, D-Latch consumes less power and considerably reduces the delay.The normal operating condition of the supply voltage is Vdd=2 V.

TABLE 1. ANALYSIS OF CURRENT MODE SIGNALING SCHEME WITH BIAS CIRCUIT AND DELAY ELEMENT

Parameter	Drain Feedback with Ring Oscillator	Drain Feedback with Inverter Delay Buffer	Drain Feedback with D-Latch	Voltage Divider with D-Latch	Voltage divider with Inverter Delay Buffer	Voltage Divider with Ring Oscillator
V_{dd}	2V	2V	2V	2V	2V	2V
Power - WO.C	1.011 mW	1.260 mW	0.627 mW	0.631 mW	1.147 mW	1.013 mW
Power - W.C	1.014 mW	1.268 mW	0.635 mW	0.640 mW	1.153 mW	1.016 mW
Frequency	510 MHz	509 MHz	504 MHz	540 MHz	521 MHz	510 MHz
Energy (mV)	100.87 mV	100.9 mV	98.58 mV	98.65 mV	106.20 mV	100.92 mV
Rise delay	0.027 ns	0.019 ns	0.020 ns	0.018 ns	0.014 ns	0.030 ns
Fall delay	0.027 ns	0.019 ns	0.020 ns	0.018 ns	0.014 ns	0.030 ns
Maximum I_{dd}	1.832 mA	2.200 mA	2.046 mA	2.046 mA	1.447 mA	1.828 mA
No. of transistors	11	11	11	11	11	11
EDP (pJ x ns)	2.724	1.917	1.971	1.776	1.486	3.027

The table 3 shows that the CMS Active bias is more efficient in terms of power and delay compared with the CMS-Fb and CMS-Smart bias.

The performance of various Current Mode signaling schemes are compared and summarized .The CMS Active bias scheme reduces power, delay and increases the speed. The system performance is improved as the rise delay and fall delay are equal.

TABLE 2 COMPARISON OF THE VARIOUS CURRENT MODE SIGNALING SCHEME

Signaling Scheme	Power (mW)	Delay (ns)	No. of transistor
CMS-Fb	1.642	0.052	14
CMS –Smart bias	2.097	0.057	20
Active bias - Drain Feedback D Latch	0.627	0.020	11
Active bias- voltage divider D-Latch	0.631	0.018	11

TABLE 3 ANAYSIS OF SIGNALING SCHEMES

Parameter	CMS-Fb Scheme	CMS-Smart Bias Scheme	CMS-Active Bias using Drain Feedback with D-Latch	CMS-Active Bias using Voltage Divider with D-Latch
Vdd	2V	2V	2V	2V
Power WO.C	1.642 mW	2.097 mW	0.627 mW	0.631 mW
Power-W.C	1.645 mW	2.103 mW	0.635 mW	0.640 mW
Frequency	2980 MHz	524 MHz	504 MHz	540 MHz
Energy (mV)	365.50 mV	483.15 mV	98.58 mV	98.65 mV
Delay	0.052 ns	0.057 ns	0.020 ns	0.018 ns
Maximum Idd	1.64 mA	2.590 mA	2.046 mA	2.046 mA
No. of transistos	14	20	11	11
EDP (mV x ns)	19.006	27.539	1.971	1.776

5. APPLICATION OF CURRENT MODE SIGNALING SCHEME

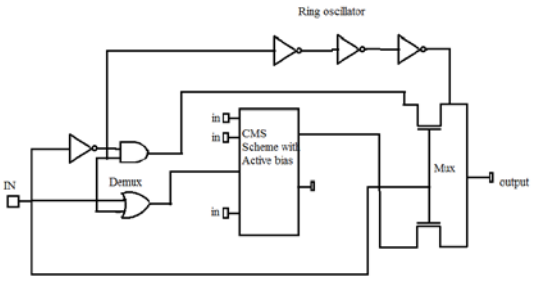

Fig 9. Block diagram of Delay measurement scheme using Active bias

The Current mode signaling scheme with active bias is implemented as the interconnect in the delay measurement scheme .Delay measurement scheme is applied using 2 X 1 Mux and Demux The input is fed at the Demux ,where the current mode signaling scheme with active bias is implemented as the interconnect, which is recovered at the Mux end without any fluctuation or state change of the data line. The delay measurement scheme produces tradeoff between power and delay[11].The power obtained, when Active bias(voltage divider with D-latch) is used in the delay measurement scheme is about 0.757 mW and delay is 0.144 ns. Similarly for Active bias(drain feedback with D-Latch),the power is about 0.902 mW and delay is 0.135 ns.

6. CONCLUSION

In Existing scheme , CMS-Fb the power consumption reduces but the delay increases. In CMS-Smart bias , the power and area increases with decrease in delay. The proposed scheme is implemented in 180nm technology In the proposed CMS –Active bias, the performance of the interconnect is improved by increasing the speed by reducing the delay and area & power consumption is been

reduced .. In CMS –Active bias, the power is nearly 70% improved.

REFERENCES

[1] Hui Zhang , Jan Rabaey , "Low Swing Interconnect Interface Circuits"UC Berkeley,1997.

[2] H.Kaul and D.Sylvester, "Low power on-chip communication based on Transition aware global signaling," IEEE Trans.Very large scale integ(VLSI) syst.,vol.12,no.5,,pp. 464-476, May 2004.

[3] H.hang, V.George,and J.M.Rabaey, "low swing on-chip signaling techniques, Effectiveness and robustness," IEEE Trans. Very Large scale integr.(VLSI)syst., vol.8,no.6,pp.264-272,Jun.2000.

[4] J.Sun.Seo, P.Singh, D.Sylester, and D.Blaauw, "Self time regenerators for high-speed and low power interconnect," in Proc.ACM/IEEE Int.Symp.Quality Electron.Design,2007,pp.621-626.

[5] A.Katoch, H.Veendrick, and E.Seevinck, "High Speed current mode signaling circuits for On-Chip wires," in proc.IEEE int.symp. circuirs syst.,200,pp.4138-4141.

[6] R.Ho,T.Ono, R.D.hopkins, A.Chow.J.Schauer, F.Y.Liu, and R.Drost, "high speed and low energy capacitively driven on-chip wires,"IEEE J.Solid state Circuits, vol.43,no.1,pp.52-60,Jan.2008.

[7] A.Nalamalpu, S.srinivasan, and W.Burleson, "Boosters for driving long On-Chip interconnects: design issues, interconnect synthesis and comparison with repeaters,"IEEE Trans.Comput –aided design Inter circuits syst., vol.50,no.4,,pp.50-62,Jan.2002.

[8] E.Mensink, D.Shinkel, E.A.M.Kulumperink ,E.Van Tuijil,and B.Nauta, "Power efficient gigabit communication cacitively driven RC-limited on-chip interconnects,"IEEE J.Solid State circuits, Vol.45, no.2,p.447-457,Feb.2010.

[9] M.M.Thabrizi, N.Masoumi, and M.M.Deilami, "high speed current mode signaling for interconnects considering transmission line and cross talk effects," in Proc.MWCAS,2007,pp.17-20.

[10] D.Shinkel, E.Mensink, E.A.M.Klumperink, E.Van Tuijl, and B.Nauta, "A 3-Gb/s/ch transceiver for 110-mm uninterrupted RC limited global On-Chip interconnects," IEEE J.Solid State Circuits, Vol.41,no.1, pp.297-306,Jan.2006.

[11] G.Nithiya Devi, J.Sathiya Priya, "An Efficient System On-Chip Interconnect using Modified Smart Bias Circuit - 2014,"International Journal of computer applications(ICIIECS)-2014.

[12] Priyadharsini.R, Mr.Mahesh Kumar.H "Effective Power Optimization Of CMS Scheme International Journal of Advanced Research in Computer and Communication Engineering" Vol.3,Issue 2,February 2014.

[13] Prabakaran J and Ravi V, "A Low Power and High Performance On-Chip Interconnect using Current Mode Signaling Scheme"International Journal of Emerging Trends in Electrical and Electronics(IJETEE)",Vol-6,August 2013,ISSN:2320-9569.

[14] S.Karthika Swathini,P.N.Palanisamy, "Efficient on-Chip Interconnects using CMS scheme with Variation Tolerant",IJAICT Vol 1,October 2014,pp 512-516

[15] M.Dave, M.Shojaei,and D.Sharma,"A Variation Tolerant Current Mode Signaling for on chip interconnects",IEEE Transaction on Very Large Scale Integration Systems,Vol.21 no. 2,February 2013.

[16] M.Dave, M.Shojaei,and D.Sharma, "energy efficient current mode singnalling scheme for o chip interconnects,"presented at the Asian Solid-Stt conf.,Beijing,china,2010.

[17] Richard, T.Chang,Nirajan Talwalkar ,C.Patrick Yue and S.Simon Wong "Near Speed-of-Light Signaling Over On-Chip Electrical Interconnects".IEEE Journal of Solid-State Circuits Vol.38,No.5,May 2003.

[18] Richard, T.Chang,Nirajan Talwalkar ,C.Patrick Yue and S.Simon Wong "Near Speed-of-Light Signaling Over On-Chip Electrical Interconnects".IEEE Journal of Solid-State Circuits Vol.38,No.5,May 2003.

[19] A.Narasiman, "A low power asymmetric source driver level converter based current mode signaling scheme for global interconnects," in Proc.IEEE Int. conf.VLSI Design,2006, pp.491-494.

[20] Alongti Longchar,N. Prameela .Kumare, "Advanced low power interconnect signaling schemes" , proc. of Int. Conf on Advances in Recent Technologies in Communication and Computing 2011.

[21] Anthony J. Walton, William Gammie, Martin Fallon, J. Stevenson, and Robert , "An Interconnect Scheme for Reducing the Number of Contact Pads on Process Control Chips", IEEE Transactions on Semiconductor Manufacturing Vol. 4, No. 3, Aug 1991.

[22] D Tran ,Kyung Ki Kim ,Yong-Bin Kim , "Power Estimation in Digital CMOS VLSI Chips".

[23] D.Liu and Christer Svensson , "Power Consumption Estimation in CMOS VLSI Chips" , in IEEE Journal of Solid-State Circuits ,Vol 29 ,No 6 1994,pp 663-670.

[24] Giacomo Paci, Davide Bertozzi, Luca Benini "Effectiveness of Adaptive Supply Voltage and Body Bias as Post-Silicon Variability Compensation Techniques for Full-Swing and Low-Swing On-chip Communication Channels" ENDIF,University of Ferrara.

[25] Hsien-Chie Cheng, Yu-Min Tsai, Su-Tsai Lu, and Wen-Hwa Chen, "Interconnect Reliability Characterization of a High-Density 3-D Chip-on-Chip Interconnect Technology" IEEE Trans. On Components,packaging and manufacturing technology Vol. 3, No. 12, Dec 2013.

[26] Jae-sun Seo,Prashant Singh, Dennis Sylvester and Dravid Blaauw " Self-timed Regenerators for High-speed and Low – power interconnect," Department of EECS ,MI 48109 .

[27] John D Owens,William J Dally,RonHo,D.N.Jay,S.W.Keckler,Jayasimha,Li-Shiuan Peh , "Research Challenges for on-chip interconnection networks" , IEEE Micro ,no.5,pp 96-108.

[28] L.Zhang, J.Wilson, R.Bashirullah, L.Lue, J.Xu,and P.Franzon, "A Gb/s on chip bus with driver pre emphasis technique for on chip buses,"in proc.custom integr. Circuit conf.2006,pp.265-268.

[29] Mandeep Bamal, Scott List,Michele Stucchi, Anne S. Verhulst,Gerald Beyer and Karen Maex, Marleen Van Hove, Rudi Cartuyvels, "Performance Comparison of Interconnect Technology and Architecture Options for Deep Submicron Technology Nodes" IEEE 2006 pp.202-204.

[30] N.Tzartzanis and W.W.Walker, "Differencial current mode sensing for efficient on-chip global signaling,"IEEE J>Solid state circuits ,vol.40,no.11,pp.2141-2147,Nov.2005.