DESIGN OF LOW POWER WITH EFFICIENT RTPG FOR BIST WITH REDUCING SWITCHING ACTIVITY

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***Abstract*—*A low power (LP) programmable generator proficient of producing random test patterns with desired toggling levels compared with the built-in-self test(BIST) based linear feedback shift register. The device to produce binary sequences with preselected toggling(PRESTO) activity is allowed by test coverage improvement is embraced of a linear finite state machine (RTPG-random test pattern generator). An LP test compression method using design for testability based on scan and automatic test pattern generation were advanced to test all gate and path in a strategy. This technique creating high-quality vector for manufacturing test ,with good test coverage. This method gives a high quality test by achieving three modes such as less repetition mode,test vector coverage, switching activity.Experimental results obtained for industrial design illustrate the possibility of the proposed test schemes and are reported herein.*

Keywords— Built-in self-test (BIST),low-power(LP) test, Random test pattern generators(RTPGs),test data volume compression

1. INTRODUCTION

Very-large – scale integration is the process of creating an integrated circuit by combining thousands of transistor into a single chip .VLSI behind in the 1970s when complex semiconductor and communication technologies were being advanced. An electronic circuit might consist a CPU , ROM ,RAM and other glue logic .VLSI lets IC designer add all of these into one chip.The primary objective of manufacture test will remain essentially the same to assure believable and high quality semiconductor products conditions and consequently also test solution may undergo a special evolution. The semiconductor technology, design characteristics, and the design process are among the key factors that will influence this evolution

LBIST (logic-built-in-self-test) is originally developed for board, system and in-field test, its result in increasing often with test compression .it has potential for improved test qualities it maydisputation the abilities to run at-speed power aware test , and it can reduce the cost of manufacturing test while preserving all LBIST and the scan compression is advantages .

The unifying LBIST and data compression is a prominent research to conquer the test data bandwidth between the tester and chip with headwayarea.In BIST design to store deterministic to detect random pattern resistant fault on the tester in a compressed form .If BIST logic is used to transport compressed test data , then underlying encoding schemes typically take advantage of low fill rates , as originally d projectedLFSR coding , which successively evolved first into static LFSR reseeding , and then into dynamic LFSR reseeding. As a conventional scan- based test, hybrid schemes,due to the high data activity associated with scan-based test operation, may consume more power than the circuit-under function.

During normal operation and capture,the logic remainsvariation on chip clock gating circuitry to selectively block scan chains. Its further decreasestheBISTpower.

vector test,often very large and high fault occur,detect the fault also. Elimination of such test can reduce switching activities with no impact on fault.

2. LITERATURE SURVEY

(A).LOWER DECOMPRESSOR AND PRPG CONSTANT VALUE BROADCAST

A low power test scheme compatible with test compression and BIST.A simple power aware controller may allow significant reductions of toggling rates when feeding scan chains with either decompressed test patterns or pseudorandom vectors.

The proposed solution requires minimal modification of existing DFT logic, its use results in a low switching activity.It reduces power consumption and helping to resolve problems related to power dissipation, voltage drop, and increased temperature.

(B).ADAPTIVE LOW POWER TEST PATTERN WITH LOGIC BIST

Increasing a correlation proximate test actuator bit can significant reduce shift power consumption.Often urge test coverage loss when applying it to reduce the shift power consumption in logic BIST.

A new adaptive low shift power random pattern generator(ALP-RTPG) to improve thecompromise between test coverage loss and shift power bargainin logic BIST .

Achieved by applying information derived from test responses to dynamically adjusted the correlation among proximate test stimulus

DERMITS:

i. Often cause test coverage loss.
ii. It reduced the shift power consumption.

(C).RESTRICT ENCODING FOR MIXED MODE BIST

Programming mixed-mode BIST design combine PRPG and deterministic test.Mixed-mode BIST design able to exploit the regularities of a deterministic test pattern horde for minimizing the hardware overhead and memory requirement.

Minimizing hardware overhead and memory requirementMixed-mode method more than 50% hardware cost compare with the best scheme known.

(D).BIT SWAPPING LFSR FOR LOW POWER BIST

A modified linear feedback shift register is used to reduce the number of mutation at the input of the circuit under-test by 25% using bit swapping technique

An experimental result on ISCA's 85 and 89 benchmark circuit up-to 45% power reducing during test.The design can unify with other technique to achieve a power reduction up-to 65%

(E).TEST GENERATOR WITH PRESELECTED TOGGLING FOR LOW POWER BUILT IN SELF TEST

This is a new pseudorandom test pattern generator with preselected toggling activity.It is comprised of a linear finite state machine driving an appropriate phase shifter and tool with a number of features that allowed device to produce binary sequence with toggling rates.

Its protecting test coverage achievable by the best-to-date conventional BIST –based PRPGs with negligible consequence on test application time.

(F).HISTORICAL PERSPECTIVE ON SCAN COMPRESSION

In recent year however technology has taken the test industry by storm.As the cost of test increasing to previously unseen height, some companies complained that the cost of test a single transistor was nearly equal to the manufacture it.

Scan compression technology, however proved to be a powerful antidote to this problem, it catalysed reduction in test data volume and test compression.As the result,the cost of test may well be contained for many years to come.This test technology exploration that has led to the stunning success of scan compression.

3. EXISTING METHOD

The LP generator is used easy implementation can produce pseudorandom test pattern with scan shifted –in switching activity is selected through automated programming. This LP PRPG is also efficient of acting as fully functional test data decompression with the ability to control scan shift in switching activities through the process of encoding .It is a very attractive LP test allows scheme that allow for trading–off test coverage, pattern counts, and toggling rates in very flexible manner .The proposed hybrid solution one to efficiently combine test compression with logic BIST, both technique can work synergistically to deliver high quality test.

For the scan chains value at the output of basic logic is depend to reduce the number of transition occur at the scan chain input.A dual speed LFSR consists of two LFSR driven by normal and slow clock respectively.

4. PROPOSED METHOD

TheRandom test pattern generator is random in nature to replace truly random sequence.It is obtained by three modes are,

i. Less repetition mode.
ii. Coverage of test patterns.
iii. Reducing the switching activity.

(a).ARCHITECTURE OF PRESTO GENERATOR BASED RTPG

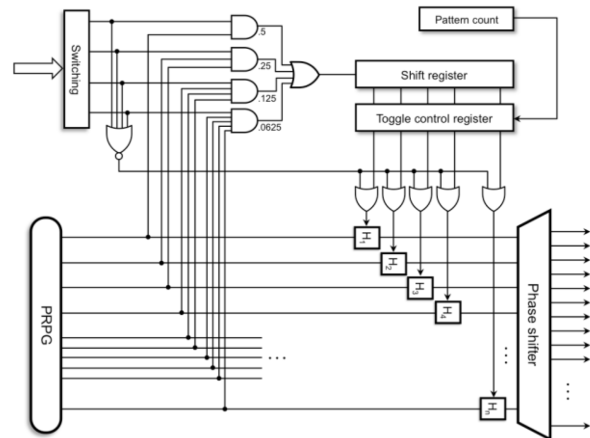

Fig.1.Architecture of PRESTO generator based RTPG.

Fig1. Shows the basic structure of a PRESTO generator.An n bit RTPG is connected with a phase shifter which suckles the scan chains producing the actual random test patterns.A RTPG is employed by a linear feedback shift register.There are n hold latches which are placed between RTPG and phase shifter.

Each separate hold latches is controlled by a corresponding stage of n bit toggle control register.When the input is enabled,the given latch is transparent for data going from RTPG to phase-shifter and in the sense it is in the toggle mode.The number of clock cycles captured and saved,when the latch is disabled and the corresponding bits of RTPG feeds the scan chains with a constant value.When now it is in the hold mode, that each phase shifter output is obtained by XOR-ing outputs of three different hold latches.The low power mode is remained in every scan chains which provides onlydisabled hold latches to the corresponding phase shifter output.

The hold latches are supervised by toggle control register.Its content is comprised of 0's and 1's,where 1's indicate latches in the toggle mode,which is transparent for data coming from RTPG.Their fraction determines the scan switching activity.The control register is added for each pattern with the additional phase shifter.

The original RTPG are produced by the enable signals injected into the shift register with programmable set of weights.The weights are determined by four AND gates producing 1's with the probability of 0.5, 0.25, 0.125 and 0.0625 respectively.The power of 2 is choose by the probabilities of OR gate.

An AND gate is activated which is employed by the 4-bit register switching and allows selecting the user-defined

level of switching activity.The shifting period splits every test pattern into sequence of alternating hold and toggle intervals.The T type flip-flop is used to move the generator front and back between these two states that switches whenever 1 on its data input.

If it sets 0,the generator will be in hold period with all latches temporarily disabled.If itsets to 1,then the latches enabled by control register which passes the test data moving from RTPG to scan-chains.A 4 bit hold and toggle register determines the entire generator remains either in hold mode or toggle mode.

This weighted random signal is produced is similar to the weighted logic used to feed the shift register.The T flip-flop controls also four 2-input multiplexers data from toggle and hold registers.This registers allows the selecting the source of control data that will be used in next cycle change the operational mode of generator.

When using of PRESTO generator with an existing DFT flow,all low power registers are loaded once per test or every test pattern.With the help of shadow registers,values remain unchanged during capture.The performance of the PRESTO generator depends primarily on the following three factors are,the switching code,the hold duty cycle(HC),the toggle code(TC).

(b).FUNCTIONAL ARCHITECTURE OF RANDOM TEST PATTERN GENERATOR

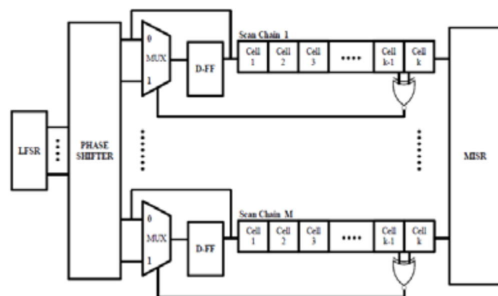

Fig.2.Functional architecture of RTPG.

Power reduction during testing is an important concern in scan based tests.But the methods to reduce shift power will result in test coverage loss.So a low power random test pattern generator(LPRTPG) is presenting to improve the trading-off between shift power reduction and test coverage loss.

To get the required trade-off,for an adaptive type technique is utilizing where the previous test responses are given as feedback to a transition controller which is capable of generating highly correlated test patterns.

The experimental results on I-SCAS'89 bench mark circuit shows efficiency of the work in terms of reduction in test power.An adaptive technique is applied to get low shift power RTPG to improve the trade-off between test coverage loss and shift power reduction in logic BIST.

To get the required trade-off,there implemented an additional hardware module named transition controller.During shift mode the previous test responses in scan flip-flops are given feedback to a transition controller which is capable of generating highly correlated test patterns so that the switching activity will reduce.

Step 1.Generate scan chains for ISCAS'89 circuit by applying DFT constraints.

Step 2.Generate netlists and ATPG files for the circuit under test.

Step 3.Find out the test coverage and generate test patterns of the bench mark circuits without transition controller.

Step 4.Modify the net list to incorporate the transition controller circuit and find out the test coverage and generate test patterns of the bench mark circuits.

5. EXPERIMENTAL RESULT

The experimental result gives the reduction of switching activity,coverage of test patterns and reduces the power and reduces the area.

Fig3Result for PRESTO generator using RTPG

Device	
Family	Virtex4
Part	xc4vsx25
Package	ff668
Temp Grade	Commercial
Process	Typical
Speed Grade	-12
Environment	
Ambient Temp (C)	27.5
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Characterization	
PRODUCTION	v1.0,02-02-08

On Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.011	11	---	---
Logic	0.000	112	20480	1
Signals	0.000	179	---	---
DCMs	0.000	0	4	0
IOs	0.000	24	320	8
Leakage	0.280			
Total	0.291			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	8.7	82.5	30.0

Supply Summary Source	Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.111	0.009	0.101
Vccaux	2.500	0.062	0.000	0.062
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.291	0.011	0.280

Fig 4. Reduction of power in PRESTO generator using RTPG

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	68	20,480	1%	
Number of 4 input LUTs	41	20,480	1%	
Number of occupied Slices	44	10,240	1%	
Number of Slices containing only related logic	44	44	100%	
Number of Slices containing unrelated logic	0	44	0%	
Total Number of 4 input LUTs	41	20,480	1%	
Number used as logic	31			
Number used as Shift registers	10			
Number of bonded IOBs	12	320	3%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Average Fanout of Non-Clock Nets	2.63			

Fig 5 Reduction of area in PRESTO generator using RTPG

Fig 6 Reduction of switching activity in PRESTO generator using RTPG

6. CONCLUSION:

Therefore, PRESTO- the LP generator can produce random test patterns with scan shift-in switching activity which is selected by automated programming.When still reducing the toggling rates down to desired levels they can suffuse higher number if run for comparable test times.

By the process of encoding the LP RTPG capable for fully functional test data decompressor which control scan shift-in switching activity.The propose method allows one to efficiently unify test compression with logic BIST which gives the high quality test.Therefore it reduces the area,power and switching activity.It gives efficient test pattern generation.

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