Implementation of Quaternary Logic Using Clock Boosting Technique for Combinational Circuit

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Abstract—*CMOS (Complementary Metal- Oxide Semiconductor) is a class of integrated circuit in which the term 'complementary' refers to the fact, of typical design style with CMOS using p type and n type metal oxide semiconductor field effect transistors for logic functions. CMOS technology is employed in microprocessor, microcontroller, static RAM and other digital logic circuits. Two major characteristics of CMOS device are high noise immunity and low static power consumption. Interconnections play an important role in delay, power and area. Hence interconnection reduction is a major concern in system integration, because it increases the area, power and delay. In this project, Quaternary lookup table and clock boosting techniques are used. The clock boosting technique is to optimize the resistance and power consumption. We design a combinational circuit using the tanner and micro wind software, simulated in a standard 120nm CMOS technology, which is able to function at 120MHz consuming 120µW. The experimental results demonstrate the correct quaternary operation and confirm the power efficiency of the proposed design.*

Keywords— full subtractor, vigor, area

1. INTRODUCTION

Arithmetic circuit design is among the predominant a part of digital circuits. The arithmetic circuits reminiscent of adder, subtractor and multiplier, etc. In digital circuits the subtractor is the essential component, which utilized in microprocessor of moveable gadgets. Area, lengthen and vigor consumption are essential consideration within the design of three-bit full subtractor. On this undertaking we introduce a brand new appear-up table constitution founded on low-vigor and high-velocity quaternary voltage mode device. The Quaternary table uses the clock boosting technique and normal CMOS technological know-how to enhance velocity without increasing energy consumption .It's going to include performing static timing analysis on the routed knowledge, opting for a record of the preferred clock delays and editing the routed knowledge to insert the favored cock delays. We reward an ASIC prototype of full subtractor established on the search for desk and experimental results are simulated .The simulation carried out utilizing the application tanner and micro wind.

2. RELATED WORK

Interconnection plays a major role in the feature of circuit design equivalent to delay, power and discipline. This create severe result in FPGA. So the interconnection will have to be limited. To beat this difficulty this assignment introduced quaternary logic. This used to be carried out by utilizing normal CMOS technology and it is founded on a voltage-mode structure [1].

Clock boosting process and general CMOS technological know-how are the most important elements of lowering the area, extend and vigor. It broaden the pace without increasing the vigor consumption.ASIC (software exact built-in Circuit) custom-made for a specified use, as an alternative than intended for a common rationale use. A single prototyping platform can provide verification for hardware, firmware and utility application design functionality before the primary silicon cross [2].

This task replaces quaternary lookup desk as an alternative of complement binary LUT in FPGA. The proposed approach clear the boundaries of quaternary implementation such as adder, subtractor, multiplier and so on.[3].

3. QUATERNARY LOGIC AND LUTS

The transistors threshold voltage (Vth) cannot be reduced proportionally to the vigor provide voltage as it results in an increasing leakage present, for that reason increasing the static consumption of CMOS circuits.

3.1 Quaternary Logic

Multivalve common sense (non binary good judgment) digital logic for use in common sense circuits that are designed to manage more than two level (voltage and many others).In q- valued common sense there are q degree and every reminiscence element(flipflop,etc.),can exists in q specific states .The classification of logic circuit in to combinational and sequential circuit. It's applied to multi worth good judgment precisely because it does to binary logic.

There's a lot curiosity currently in ternary logic(q=3)to a somewhat lesser extent, in quaternary good judgment(q=4).Such logics guarantees to lower numbers in good judgment gates ,reminiscence detail and possibly most vastly interconnection ternary common sense simple to enforce in CMOS technological know-how and is likely to be predominant in design of VLSI circuit. It's multiplied logical richness is proven by way of incontrovertible fact that there are sixteen viable two input binary gates, but

1968 $_3$such ternary gates (ignoring degeneracy in both instances).

A quaternary variable (Q) is able to carry twice as much information as a binary variable (B), we have the following relation:

$$|Q| = 2 \times |B|. \quad \text{-------1}$$

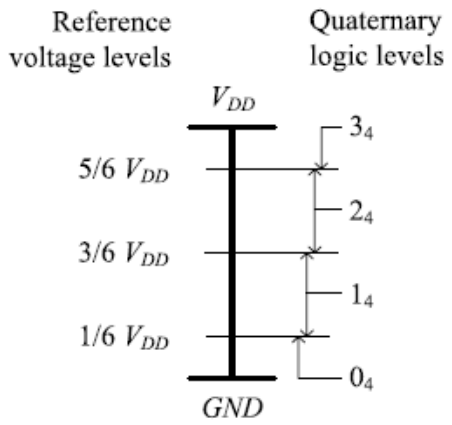

Fig 3.1 Quaternary logic and reference voltage level

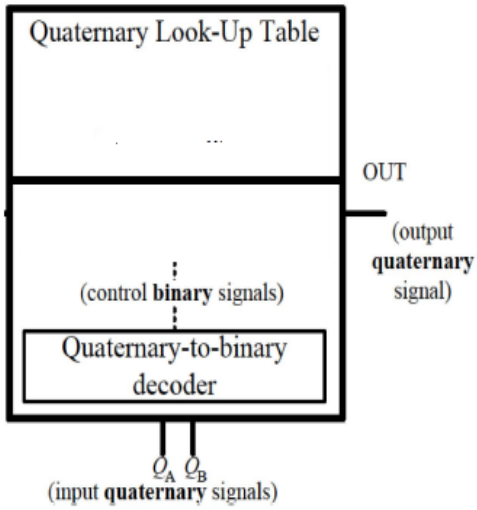

Fig 3.1.2 Proposed quaternary LUT

3.2 Lookup Table (LUT)

The seam up table is the common proposal use to scale back processing time for software that uses intricate calculation. Clearly the LUT includes data or results from the elaborate calculation wanted by means of software which was once achieved earlier than hand –ones. By way of retaining results in LUTS, when the applying desires the worth rather having to do the calculation. It's complicated software akin to sign processing, photograph processing, gadget modeling elaborate calculation are used repeat and utilizing the LUT help significantly by vastly cut back the processing time.LUT is meant in to be used robotic action manipulate method.

3.3quaternary-To-Binary Decoder

The 4-bit quaternary-to-binary decoder allows the use of a single row of switches to drive the input configuration signals to the output of the QLUT. To do so, it is necessary to generate 16 control signals, to be applied in the clk1 inputs of each switch, shown in .These switches are employed to connect one quaternary configuration input to the output. To generate the required control signals, the quaternary variables are decoded into binary, allowing the use of binary logic gates. Thus, an ADC frontend is necessary, considering the analog nature of the quaternary signals. We have implemented inverting self-referenced comparators, where Qi is a quaternary input of the QLUT. The main advantage of this structure, also used in [4], over previously proposed implementations are that it only uses standard CMOS structures. The ADC front end, where the binary signals.

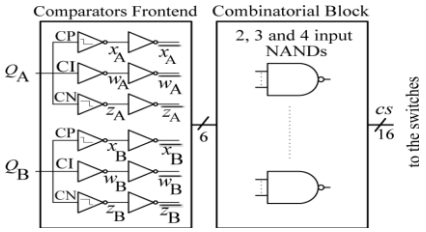

Fig 3.3.1 Proposed quaternary-to-binary decoder high-level model.

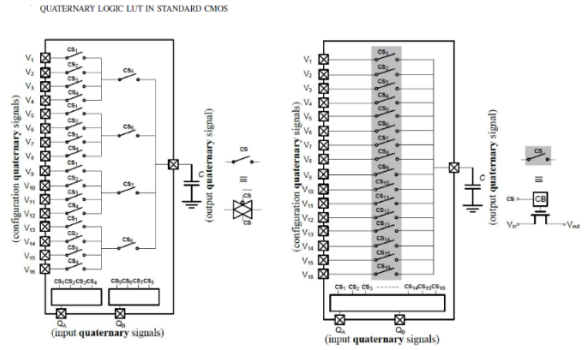

Fig 3.3.2) previous method b) proposed method

3.4 Clock Boosting Technique

The CB circuit is obtained through reasoning on the excessive degree units, the place the two operation phases of the process are depicted: in phase 1, the capacitor C is charged to VDD, and the swap (an nMOS transistor) is open in view that its gate is attached to floor; in segment 2, C is disconnected from the voltage provide, keeping its charge, while the bottom plate is referenced to VDD. For this reason, the switch gate voltage is raised to 2VDD. This excessive level circuit is as a rule carried out simply via replacing the switches by means of TGs and relying on a clock generator circuit to manipulate its phases, which, depending on the implementation, may just need to be non-overlapped. This inverter can be utilized to delay the sign at the same time simultaneously imposing the non-overlapping clock used to control the opposite switches. The entire circuit can now be lowered to the circuit in that works as follows: assuming that the capacitor C is at the beginning discharged and clk1 is about to logic 1 (VDD), N1 activates and connects node B to floor, at the same time P1 turns off and ensures a excessive impedance direction between the nodes A and B. Simultaneously, P2 is on and gradually expenses the capacitor (and node A) to VDD.

When clk1 commutes to a good judgment 0 (floor), N1 turns off; the inverter ties the capacitor backside plate to VDD and P2 turns off; node A rises to 2VDD and P1 is grew to become on connecting node B to 2VDD as desired. In observe, a somewhat decrease voltage is acquired because of cost redistribution with the transistor NSW gate capacitance. This small voltage drop prevents the transistor from working underneath a gate voltage close to the highest voltage allowed for the technology (2.7 V), heading off untimely aging effect on this colossal transistor. Additionally, due to the fact that we're making use of a greater voltage than provide to the drain-supply of the transistor N1, we are also compromising its long run use. Nevertheless, a answer for this crisis is to make use of an nMOS in series with N1, avoiding the drain-supply voltage to be bigger than VDD, in each transistor. It should even be famous that a full charge of this capacitor handiest happens once at powering up, from then on the capacitor most effective loses charge because of charge distribution with the switch gate capacitance.

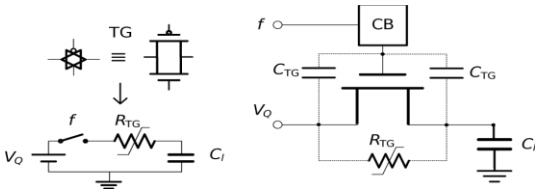

Fig 3.4 A) Multiplexer path RC model. (B) CB switch.

4. SUBTRACTOR

A subtractor performs subtraction which is without doubt one of the four normal binary operations. In lots of computers and different forms of processors, subtractor are used not just for the arithmetic calculations, but are also frequently utilized in other materials of the processor

4.1 Half Subtractor

A conventional 1/2-subtractor circuit is a combinational circuit that can be used to subtract one binary digit from one other to produce a difference output and a Borrow output. Functionally, the 1/2 subtractor consists of a 2 input XOR Gate, an INVERTER and a 2 enter AND gate. The proposed half subtractor is consist clock boosting technique

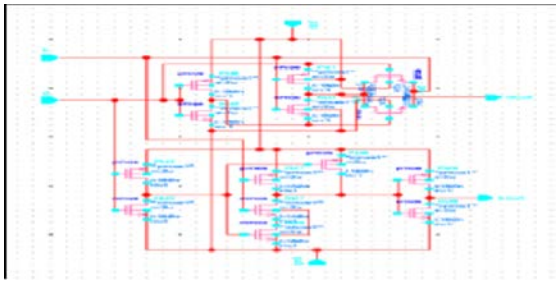

Fig4.1 Schematic of transistor level 4 bit Half Subtractor in tanner

The above figure is halfsubtractor circuit. Its consist of 2 inputs and 2 outputs. clock boosting technique is used to provide the desired clock pulse in the circuit.

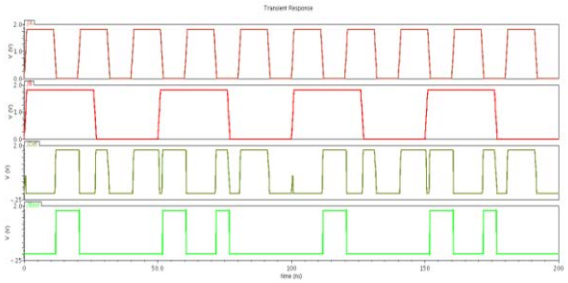

Fig 4.1.2Transient responses of proposed 4 bit halfsubtractor

Fig 4.1.2. The first and second wave forms represents input signal a&b respectively. The third output wave form represents difference and the fourth output wave form represents borrow.

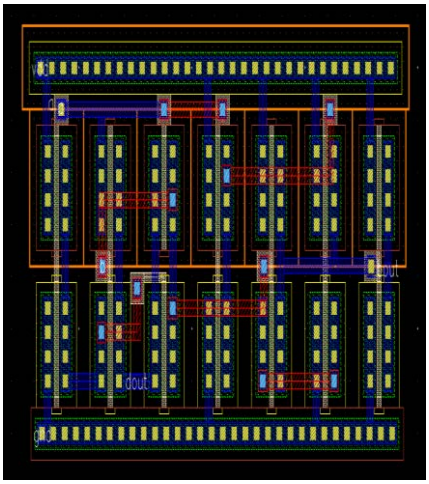

Fig 4.1.3 Layout design for half subtractor

Fig 4.1.3, The layout of half subtractor is designed using CMOS 120nm technology .The implemented layout of 4-bit half subtractor in cadence layout window are shown.

TABLE-1 Half subtractor logic function

A	B	DI	BO	A	B	DI	BO
0	0	3	0	2	0	1	0
0	1	2	1	2	1	0	0
0	2	1	1	2	2	3	1
0	3	0	1	2	3	2	1
1	0	0	0	3	0	2	0
1	1	3	1	3	1	1	0
1	2	2	1	3	2	0	0
1	3	1	1	3	3	3	1

4.2 Full Subtractor

Full Subtractor is a combinational circuit that performs a subtraction between two binary bits and1‟ can have been

borrowed by way of a scale down big stage. Let the three inputs be A, B and C. Outputs are borrow and change

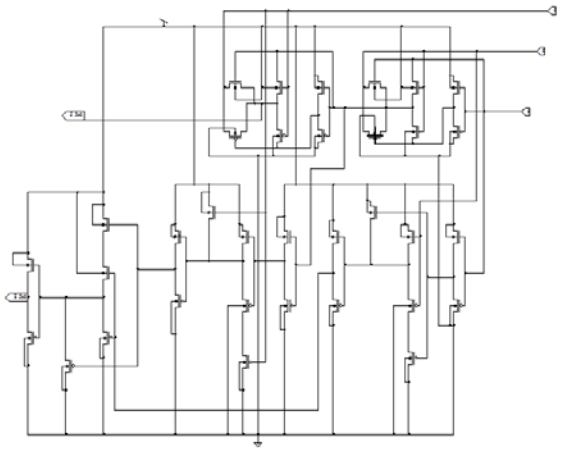

Fig 4.2 Schematic of transistor level 4 bit full Subtractor in tanner

The above figure is full subtractor circuit. Its consist of three inputs and two outputs. The three inputs are a, b,c and two outputs are difference,borrow.The clock boosting technique is used to provide the desired clock pulse in the circuit.

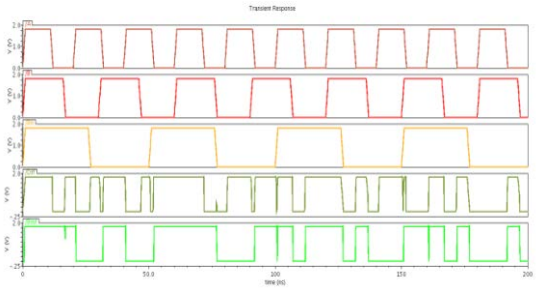

Fig 4.2.2Transient responses of proposed 4 bit full subtractor

Fig 4.2.2. The first, second and third wave forms represents input signal a,b&c respectively. The fourth output wave form represents difference and the fifth output wave form represents borrow

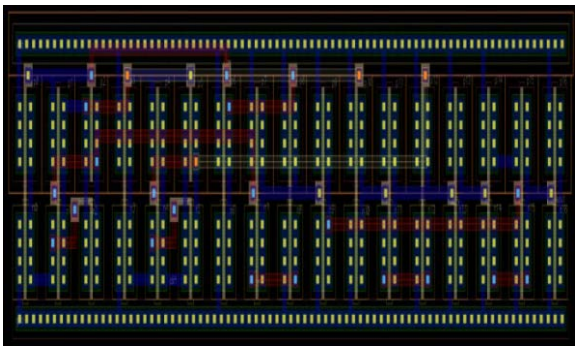

fig 4.2.3Layout design for Full subtractor

The layout of full subtractor is designed using CMOS 120nm technology as shown in Fig 4.2.3

TABLE-2 Full subtractor logic function

A	B	C	DI	BO	A	B	C	DI	BO
0	0	0	0	0	0	0	1	3	0
0	1	0	1	1	0	1	1	2	1
0	2	0	2	1	0	2	1	1	1
0	3	0	1	1	0	3	1	0	1
1	0	0	1	0	1	0	1	0	0
1	1	0	0	0	1	1	1	3	1
1	2	0	3	1	1	2	1	2	1
1	3	0	2	1	1	3	1	1	1
2	0	0	2	0	2	0	1	1	0
2	1	0	1	1	2	1	1	0	0
2	2	0	0	0	2	2	1	3	1
2	3	0	1	1	2	3	1	2	1
3	0	0	3	0	3	0	1	2	0
3	1	0	2	0	3	1	1	1	0
3	2	0	1	0	3	2	1	0	0
3	3	0	0	0	3	3	1	3	1

5. SIMULATION RESULT

The power, delay of previous method and proposed method given below

TABLE-3 Delay and power summery of pervious method

Logic gates	Number of transistor	delay	Power
half subtractor	24	134ps	18
Full subtractor	40	280ps	48

TABLE-4 Delay and power summery of proposed method

Logic Gates	Number of transistor	delay	Power
half subtractor	14	124ps	17.04
Full subtractor	34	270ps	47.5

6. CONCLUSION

Total, on this test distinctive capabilities and procedures had been received and utilized in a principal part. Certainly, we can be competent to design, implement and effectively analyze the characteristics of a 4-bit full subtractor circuit. The completion of this major undertaking was ample given that the theoretical expectations matched our experimental outcome. The efficiency of the 4-bit full subtractor was assessed in terms of field, speed and energy consumption, additionally best of the output signals by means of evaluating the timing measurements of each circuit by means of the propagation delays. The total extend and energy utilized in proposed 4 bit full subtractor compared to traditional 4 bit subtractor

REFERENCES

[1] D. Brito, J. Fernandes, P. Flores, and J. Monteiro, "Design and characterization of a QLUT in a standard CMOS process," in Proc. IEEE 19th ICECS, Dec. 2012, pp. 288–291.
[2] R. Cunha, H. Boudinov, and L. Carro, "Quaternary look-up tables using voltage-mode CMOS logic design," in Proc. 37th Int. Symp. Multiple-Valued Logic, 2007, pp. 56–58.
[3] J. Kim, "An area efficient multiplier using current-mode quaternary logic technique," in Proc. 10th IEEE Int. Solid-State Integr. Circuit Technol.,Nov. 2010, pp. 403–405.
[4] W. S. Chu and W. Current, "Current-mode CMOS quaternary multiplier circuit," Electron. Lett., vol. 31, no. 4, pp. 267–268, 1995.
[5] K. Current, "Current-mode CMOS multiple-valued logic circuits," IEEE J. Solid-State Circuits, vol. 29, no. 2, pp. 95–107, Feb. 1994.
[6] Neil H.E. Weste, Davir Harris," CMOSVLSI Design: A Circuits and System Perspectives" Addison Wesley – Pearson Education, 3rd Edition, 2004.