IMPLEMENTATION OF HIGH SPEED QSD ADDER FOR VLSI APPLICATION

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Abstract*—In all signal processing applications the main problem faced by the processor is its propagation delay. It makes the process to be tedious. Conventionally The Binary signed numbers(BSD) were used to overcome this problem,(BSD's) are known for its carry free addition and borrow free subtraction, but the addition process is more complicated when the number of bits is increased. Some of main problems in BCD's are they provide less storage density and large complexity. The main aim of this project is to design a efficient adder that solves the above problems with the use of Quaternary signed digit number system. The Quaternary signed digit number provides carry free addition with high storage capacity.QSD is represented by a number from -3 to +3.Carry free addition of higher bit numbers with constant delay and less complexity is possible by QSD number system. So that the speed of the processor is increased. It is simulated by using Xilinx tool 14.1 ISE.*

Keywords— Signed digit number system, Binary signed digit number system, Quaternary signed digit number system.

1. INTRODUCTION

Now-a-days adders are mostly used in various electronic applications such as Digital signal processors and computing devices these adders are used to perform various algorithm like FIR,IIR etc. Arithmetic addition, subtraction and multiplication also suffer from various problems including limited number of bits, propagation time delay, and circuit complexity. The speed of digital processor depends heavily on the speed of adders. The important things to be noted is its area, power and speed requirements. The delay experienced by any adder is due to its carry chain. In past the major problem faced by the VLSI designers is to reduce the area, and also to increase the speed of the system. But now it is possible with a use of microprocessors. The basic adders used in microprocessors is ripple carry adder.

The main disadvantage of ripple carry adder its propagation of carry bits . While performing the several arithmetic operations such as addition, subtraction and multiplication, the speed of modern computers are limited because of carry propagation delay. The carry free addition is possible only for redundancy of bits by the use of signed digit number systems. The key for high speed computation is to reduce the addition time for signed digit numbers. The time taken for addition should be constant independent of the length of the bits. Thus the addition time for the bits can be reduced, If the addition time is reduced then the speed of the processor gets increased.

Binary Signed Digit number representation provides limited carry propagation delay so that the it provides high speed operation. But the process provides limited delay with complex addition process. Quaternary signed digit number representation is a higher radix based representation that provides carry free addition and borrow free subtraction with high storage density and high speed The number representation of QSD is from {-3 to +3} .Carry free addition and other operations on a large number of digits such as 32, 64,128 or more can be implemented with constant delay and less complexity. Since the addition time of the adder is constant the speed of the adder is increased. In this paper we are going to design and compare ripple carry adder, carry select adder and a QSD adder for 32 bit.

2. LITERATURE SURVEY:

An Adder or summer is a electronic circuit that performs addition of numbers, adders are not only used in arithmetic logic units, but also in other processors where addition and other increment and decrement processes are required. The adders used in this paper are ripple carry adder, carry look ahead adder and carry select adder. Ripple carry adder uses 1 bit full adder, it produce arithmetic sum of binary number. Here each full adder inputs Cin, which is the output of previous adder. And If the number of inputs increase, more amount of delay will occur in RCA. Ripple carry adder occupies less area. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder.

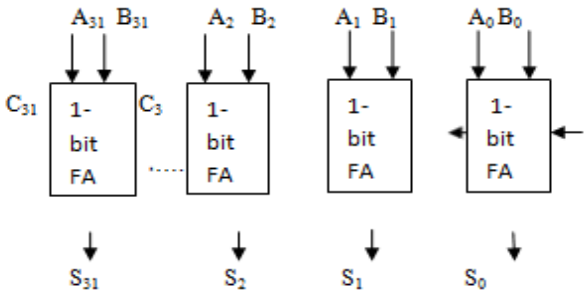


Fig:1 Ripple carry adder

The processing of full adder requires a carry, in ripple carry adder, the full adder used has to wait for the carry from the previous adder. It has to wait until the carry from the previous full adder is generated.so that the waiting time for the carry goes on increases as the number of inputs gets increased.this is said to be the Carry select adder is a particular way to implement an adder, it computes the sum of two bit numbers. This adder is simple and fast. it generally consists of two ripple carry adders and two multiplexers. In this adder there is no need to wait for carry in every stage, once the carry is known immediately the result can be obtained with low delay. The operation of carry select adder is, here we have two full adders and two multiplexers. Adding of two n-bit adders is done 2 steps, In first step the carry is assumed to be 1 and other time the carry is assumed to be 0.After obtaining the two results, the correct sum and as well as correct carry, is selected with the use of multiplexer. It is 40% to 70% faster than ripple carry adder.

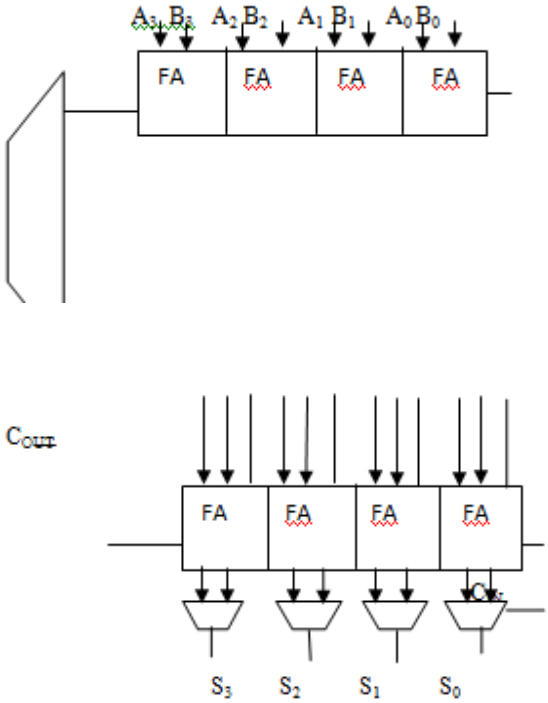


Fig 3.carry select adder

3. PROPOSED SYSTEM

QUATERNARY SIGNED DIGIT NUMBER REPRESENTATION:(QSD)

In order to overcome the disadvantages of existing system ,we are moving to a system called Quaternary signed digit number system(QSD).It is a base 4 redundant number system. The digit set of QSD numbers is{3,2,1,0,-1,-2,-3},Generally signed digit decimal n umber D can be represented in terms of an n digit quaternary signed digit number as

$$D=\sum_{n=1}^{i=0} x_i 4^i$$

where X can be any value from {-3,-2,-1,0,1,2,3}.

OPERATIONAL BLOCK DIAGRAM OF QSD:

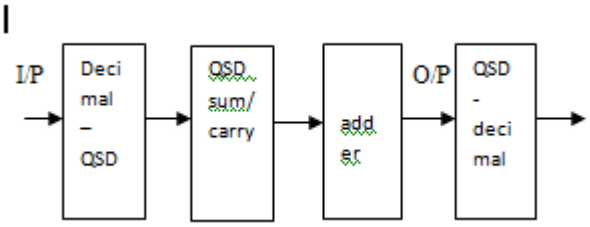


Fig 4: Block diagram representation of QSD

As shown in figure, in first step decimal number is converted to QSD. And then carries and sum are generated in step 2 further addition continues as a result it is converted to decimal system.

To prevent the carry bit propagating from lower digit position to higher bit position this system is used. Here the LSB represents the sum bit and MSB represents the carry bit. The addition of QSD numbers involves 2 steps

STEP1: It creates a intermediate carry and intermediate sum from input digits.

STEP2: Here the intermediate sum is combined with the intermediate carry, The addition process involves 2 stages are to be followed, first stage involves generation of intermediate sum and carry. And in the second stage adds the intermediate sum with the intermediate carry. In order to remove rippling of carry, further two rules are followed, they are

Rule1:The magnitude of the intermediate sum must be less than or equal to 2 i.e., it should be in the range of -2 to +2.

Rule2:The magnitude of the intermediate carry must be less than or equal to 1 i.e., it should be in the range of -1 to +1.

The range of QSD is from -3 to +3 (i.e)the numbers used are from{-3,-2,-1,0,1,2,3}.

The selected pair of intermediate carry and sum for the numbers from-6 to +6:

NO	6	5	4	3	2	1
CODE	12	11	10	1$\bar{1}$	02	01

NO	$\bar{6}$	$\bar{5}$	$\bar{4}$	$\bar{3}$	$\bar{2}$	$\bar{1}$	0
CODE	$\bar{1}\,\bar{2}$	$\bar{1}\bar{1}$	$\bar{1}0$	$\bar{1}1$	$0\bar{2}$	$0\bar{1}$	00

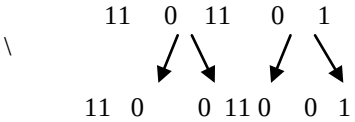
QSD CONVERTION:

1-digit QSD can be represented by one 3-bit binary equivalent as follows:

Quaternary signed digit number	Binary representation
-3	101
-2	110
-1	111
0	000
1	001
2	010
3	011

Since the sum is between -2 to +2,it requires only a 3 Binary bit and the carry is between -1 to +1 so it requires 2 binary bits for its representation. Negative numbers can be represented by its 2's compliment in binary. To convert

the n-bit binary data to 3q-bit QSD data ,we have to split the 3rd, 5th , 7th bit (i.e) the odd bits from the LSB to MSB into two portions. The MSB cannot be splitted . If the odd bit is 1 then it is split into 1&0,and if the odd bit is 0 then the splitting is 0&0.
For example:



By using this logic an adder is designed whose power and delay are reduced compared with the other adders.

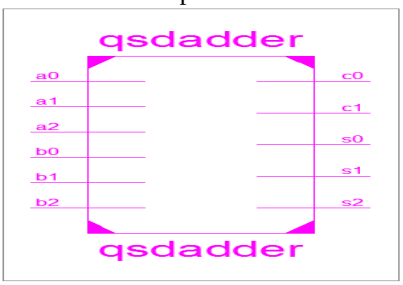
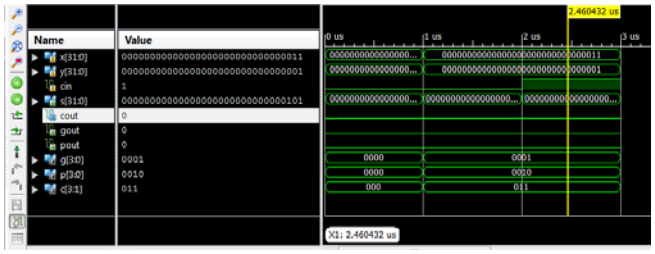


Fig 5:QSD adder

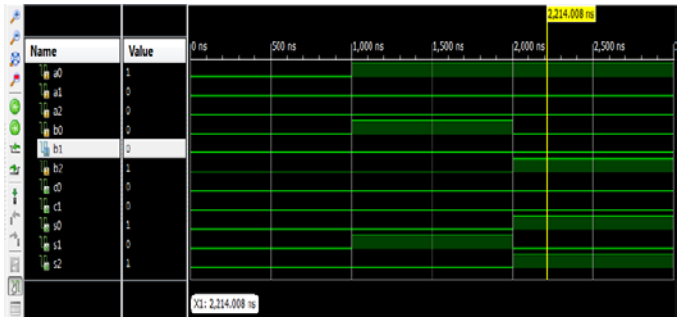
4. RESULT :

Simulation result of 32 bit ripple carry adder:

Simulation result of carry select adder:



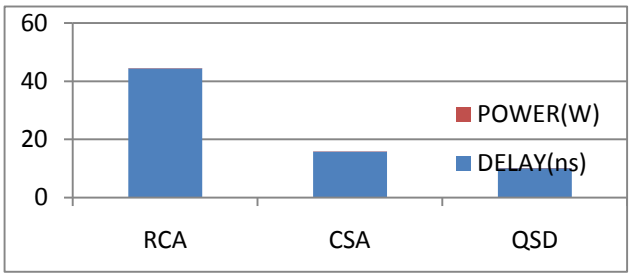
Simulation result of QSD adder:



5. CONCLUTION

ADDERS	DELAY	POWER DISSIPATION
Ripple carry Adder	44.366 ns	0.049W
Carry select adder	15.76ns	0.054W
QSD adder	10.113 ns	0.0485 W

COMPARISION CHART:



Now a days Ripple Carry Binary Signed Adders (RBSD) and Carry select Adders (CSA) are used in Arithmetic Logical Unit (ALU). The performance of these adders is limited by their computation method. Thus Designing the adder using QSD number representation allows fast addition/subtraction which is capable of carry free addition and borrow free subtraction because the carry propagation chain are eliminated, hence it reduce the propagation time, thus enhancing the speed of the system. These circuits consume less energy and power, and produce better performance. The proposed QSD adder is better than other binary adders in terms of number of gates and higher number of bits addition within constant time.. QSD number uses 25% less space than BSD, higher number of gates can be used for further improvement of QSD.

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