A NOVEL CONTROL SCHEME FOR HYBRID ACTIVE NEUTRAL POINT CLAMPED FLYING INVERTER

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Abstract*—Integration of wind energy sources into the distribution grid disturbs the voltage profile that could be stabilized through the grid reinforcement or limiting the active power injection. Furthermore a multilevel control strategy was proposed for three-phase three-level grid-connected converter based wind energy system, where the external level controller was responsible to determine the active and reactive power interchange to grid. However, an increase in the number of levels of the conventional multilevel converters increases the complexity in controlling the voltage across the dc-link capacitors of Neutral point clamped converter; the capacitors of the flying capacitor (FC) converter and the number of isolated power supplies of the cascaded H-bridge converter. A hybrid five level multilevel converter referred as FC based active-neutral-point-clamped (ANPC) converter is considered. The redundant switching states of the FC based five-level ANPC converter are consumed to control the voltage across FC and the dc-link capacitor voltages which is achieved by simplifying the modulation of the converter. The proposed FC control strategy provides extra choice to regulate the dc-link capacitor voltages with dc offset injection technique. Simulation results are provided to verify the performance of the converter for medium voltage applications.*

Keywords*—*Multilevel Inverter;Modulation Techniques;Flying Capacitor based Active Neutral Point Clamped converter;Matlab Simulation Results

1. INTRODUCTION

Multilevel inverters have picked up enthusiasm amid the last three decades because of the expanding interest for medium to high voltage converters for an assortment of high power applications. Different topologies have been proposed to fit the requirements of distinctive applications. For medium voltage inverters, cascaded H-connect (CHB), impartial point clipped (NPC), and flying capacitor (FC) are the essential topologies.Among them, NPC and FC give a typical dc-connect which is a strict requirement for some applications [1] - [6].

FC inverter utilizes capacitors to produce yield voltage levels. The accessibility of intra-phrasal excess states in this topology can give both capacitor voltage adjusting and power misfortune conveyance among switches [7]. However, increased numbers of flying capacitors at more elevated amounts that increases the underlying expense and support extra charges and decreases the unwavering quality of the inverter alongside the capacitor pre-charge in a few applications are the primary downsides of this topology [8].

Multilevel topologies give a cunning method for associating switches in arrangement, accordingly empowering the handling of voltages that are higher than the gadget rating. The business requirement for medium voltage drives has activated considerable research in this field, in which most applications incorporate drives for pumps, blowers, compressors, transports, and the like. By and large, multilevel converters are compelling method for decreasing consonant twisting and dv/dt of the output voltages, which makes this innovation pertinent to utility interface and drives.

There are a set number of topologies that give multilevel voltages and are reasonable for medium voltage applications. The most known topologies are the unbiased point-braced NPC, the FC, and the cascaded H-connect multilevel converters. Different topologies, for example, the mixture converters have been proposed also, yet they are not completely acknowledged for modern applications. The NPC multilevel converter is a Characteristic expansion of the three-level converter introduced by Nabae (NPC3L). As can be seen, the multilevel NPC converter requires numerous clasping focuses to blend the different voltage levels over the yield. The Disservice of different clasping focuses is a confinement on the maximum adjustment list that is permitted with dynamic energy to guarantee voltage sharing over all the dc connects capacitors. Another downside of the multilevel NPC converter is the requirement for arrangement association of the clamping diodes.

NPC inverter utilizes diodes to cinch the voltage levels generated at the dc-interface capacitors to the yield. Excessive number of diodes, unequal operation of dc-connection's voltage divider capacitors, and uneven dispersion of misfortune among switches are significant issues of this topology. Space vector algorithms are accessible to lighten the lopsided misfortune and capacitor voltage issues in view of the inverter's operating condition

[5]. Dynamic NPC (ANPC) enhances the misfortune dispersion of NPC by supplanting diodes with dynamic switches providing elective unbiased point way [9].

Half breed topologies are practical arrangements where higher number of levels is required. Consolidating the points of interest of CHB, FC, and NPC, half breed inverters can give misfortune and voltage adjusting while keeping the quantity of components low. Examples of hybrid topologies combining FC and NPC can be found in [10]–[12], some of which has already found industrial applications. The 5-level FC-ANPC is a case of hybrid topologies that advanced toward the business. TheACS2000 group of medium voltage drives, popularized by ABB, utilizes this topology with both dynamic and aloof front end configurations. The primary favorable position of this topology is the use of a solitary flying capacitor to create the yield five levels. Compared to different topologies that give a typical dc-link, FC-ANPC has given a satisfactory tradeoff between the cost, execution, and dependability for 5-level applications. The disadvantages of FC-ANPC are high number of switches, series association of high voltage switches, and poor loss distribution [13].

This paper proposes another 5-level half and half topology based on FC and NPC inverters. The objective of the proposed topology is to defeat the weaknesses of the customary FC-ANPC. Thus, relatively, the proposed topology gives better loss conveyance, keeps away from direct arrangement association of high voltage switches, and wipes out 2 switches per stage leg. These focal points come at the cost of an extra capacitor and 6 diodes. All things considered, the lifetime of every capacitor is expected to draw out because of the half cycle operation and lower RMS current.

2. CONVENTIONAL SYSTEM TOPOLOGY

The existing topology incorporates a dc-connection that is common among the three stages. The dc-interface gives three voltage levels +2E, 0, and - 2E for the stage legs. Every one of the segmentsis shown in the figure 1. All the components shown in the figure have square with working voltage E i.e. one fourth of the dc-interface voltage VDC. The flying capacitors CA1 and CA2 are controlled to remain charged at the objective voltage E.

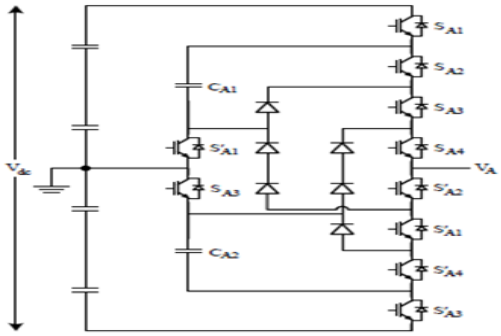


Fig. 1: A phase leg of the existing 5-level cross breed topology.

TABLE I. SWITCHING STATES OF THE CONVENTIONAL INVERTER

	State	S1	S2	S3	S4	C1	C2
+2E	+2E	1	1	1	1	N.A	N.A
+E	+EP	1	0	1	1	i>o charge i<o discharge	N.A
	+E0	0	1	1	1	i>o discharge i<o charge	N.A
0	0	0	0	1	1	N.A	N.A
-E	-E0	0	0	1	0	N.A	i>o charge i<o discharge
	-EN	0	0	0	1	N.A	i>o discharge i<o charge
-2E	-2E	0	0	0	0	N.A	N.A

S′1, S′2, S′3, S′4 are switched complementary to S1, S2, S3, S4 respectively.
i>0 represents outbound current and i <0 represents inbound current.
N.A. stands for Not Affected
The available states of one phase leg are shown in table I.To create level 2E, the entire top arm switches SA1, SA2, SA3, SA4should turn on. For level E, two decisions are accessiblei.e. either through dc-connection's certain point (EP) or through dc-link's neutral point (E0). This repetition can be utilized to adjust the voltage of CA1. Level 0 is created through clipping the dc link's neutral indicate the yield (00). Negative states can be generated likewise because of the symmetry of the topology.

The operation of this topology is fundamentally comparative to topologies, for example, stacked multicell (SMC) converter [14], [15], [7], where the positive and negative stacks operate independently. Thus, the positive stack capacitor CA1 is used and adjusted amid the positive cycle and rest amid the negative cycle, though the negative stack capacitor CA2 is used and adjusted amid the negative cycle and rest amid the positive cycle.

In this way, the flying capacitors will see the switching frequency as opposed to line recurrence and along these lines the capacitor size is not very large. Similar to the three-level NPC inverter, if the three phases of the heap are adjusted, the impartial point voltage will be constant in principle. Be that as it may, the voltage may somewhat drift away because of the irregularity in the components' spillage current. In addition, albeit little, there is constantly some imbalance among the stages.

A consistent voltage float, despite the fact that small, can cause higher voltage crosswise over part of the gadgets which can be deadly. By and by, this float can be repaid by injecting a little basic mode to the three phases. A critical element of the proposed topology is the even distribution of moves among exchanging gadgets. Therefore, switching misfortune which is the significant restricting component of inverter's thermal execution is appropriated among the switches. As the main result, the tradeoffbetween exchanging recurrence and current derating is moved forward. This gives the open door to either increment the appraised current and force of the inverter or increase the

exchanging recurrence bringing about lower capacitor size and enhanced voltage waveform quality.

3. MODULATION TECHNIQUES

Different regulation methods might be adjusted for the proposed topology. Bearer based tweak with sinusoidal or altered reference and in addition non-transporter based methods, for example, space vector regulation and particular consonant disposal might be utilized to produce the door signals. The decision of a regulation strategy is for the most part a tradeoff among the necessities of the application, many-sided quality of the product, and cost of the control equipment.

3.1 Carrier-Based Modulation:

Carrier set's course of action and reference waveform's shape are the primary wellsprings of assortments in transporter based regulation strategies for multilevel inverters. With respect to transporter set's course of action, level moved bearers LSC and stage moved transporter's PSC are the two principle classifications that are separately appropriate for diode-clipped and multi-cell structures.

Two individuals in the LSC family, elective stage restriction manner APOD and stage mien PD are known to produce the best results for scorch stage and three phase applications, separately. PSC in its unique frame has been appeared to produce a PWM waveform that matches with APOD. Additionally, an adjusted variant of PSC with element stage move has been appeared to coordinate with PD. Also a modified version of PSC with dynamic phase shift has been shown to match with PD [16].

The reference for single-stage applications is generally a straightforward sinusoidal waveform. For three-stage applications, an assortment of reference waveforms is accessible because of the likelihood of regular mode infusion in three-stage structure. This adaptability has been utilized to fill distinctive needs, for example, expanded dc interface usage, bring down THD, bring down Loss, and impartial point voltage control.

For the proposed inverter, a cross breed regulation system is required because of the mixture structure of the topology. Figure 2 represents the adjustment strategy for single-stage case. It is Intuitive to isolate the operation to positive and negative cycles, since every cycle is produced with a 3-level FC stack. The door signals for each FC is then produced utilizing PSC to give characteristic voltage adjusting to the flying capacitors. The created yield PWM waveform coordinates the APOD plot.

For three-stage case, comparative approach might be embraced aside from that, to produce a PD conspire identical, the positive cycle bearers ought to have $\pi/2$ stage move contrasted with then negative cycle transporters. Likewise, the bearers fuse a dynamic stage move which for tested reference waveforms dependably includes by $\pi/2$ at the transporter band moves. For the reference waveform, focused space vector PWM (CSVPWM) inspected at half PD bearer period can give comparable yield execution as SVM. Figure 3 illustrates the modulation technique using sampled CSVPWM along with modified PSC for the proposed inverter.

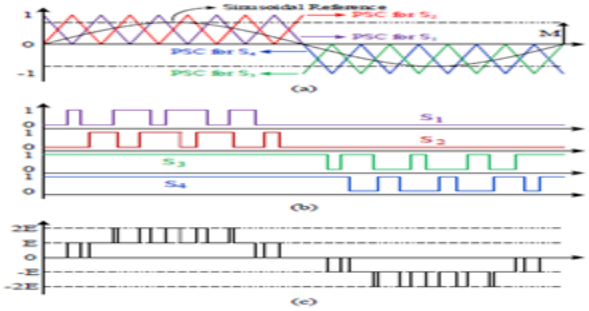


Fig. 2. Carrier-based modulation using PSC with sinusoidal reference for single phase application. (a) Reference and carriers arrangement. (b) Gate signals. (c) Output waveform.

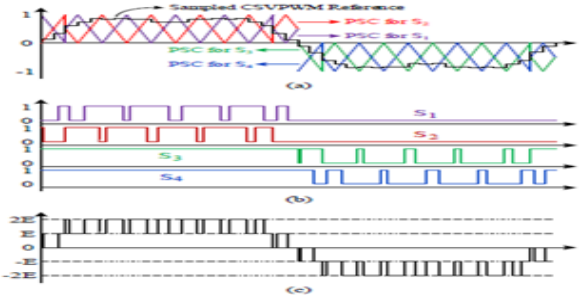


Fig 3. Carrier-based modulation using modified PSC with sampledCSVPWM reference for three phase application. (a) Reference and carrier'sarrangement. (b) Gate signals. (c) Output waveform.

3.2 Non-Carrier-Based Modulation:

For non-transporter based balance methods, for example, SVM and SHE, the yield PWM waveform might be produced first and afterward decayed to the required exchanging signals. Figure 4 delineates the obliged technique to produce the door signals for every stage leg. The 5-level PW waveform is initially isolated to positive and negative cycle 3-level PWMs.

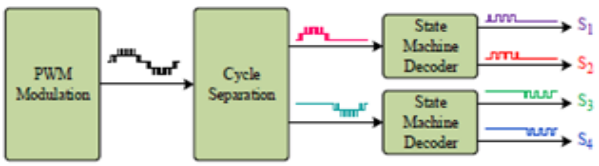


Fig. 4. Non-carrier-based modulation for a phase leg of the conventional inverter.

Utilizing state machine decoder, every cycle is then decayed to two 2-level PWMs i.e. the required entryway signals for each FC cell. Note that this strategy is free of the embraced regulation method. Accordingly, it can be utilized with transporter based adjustment methods and non-bearer based. This may be a decent option when the multifaceted nature of the bearer based procedure is generally high e.g. for PD plot.

4. THE PROPOSED TOPOLOGY AND ITS OPERATION

One needs to understand that three skimming capacitors add unreasonable cost to the general framework, and require space for accommodating the whole volume.

Hence, it is of most extreme significance to lessen the quantity of floating capacitors in the topology. This can be accomplished by further taking out C2 and C3 from the circuit, as appeared in Figure7 (a). Truth be told, the converter arrangement appeared in Figure 7 (a) is like the ANPC3L converter previously discussed. The distinction here is the vital association of the drifting capacitor that makes it conceivable to upgrade the quantity of levels from three to five. In spite of the fact that the disposal of the drifting capacitors C2 and C3 from Figure 6 (a) disentangles the circuit and cuts the cost down, it likewise dispenses with the ability to actually adjust the voltage crosswise over C1 by utilizing the transporter based PWM beat design portrayed in Figure 6 (b). By the by, such drawback is overcome by utilizing the excess exchanging states created by the converter of Figure 7 (a) to adjust the voltage across the skimming capacitor.

The arrangement association of the changes S5 to S8 is required to keep up the voltage rating for all switches at the same level. The quantity of levels can be expanded by including switches in arrangement and by expanding the quantity of cascaded two-level inverters, as represented for a seven-level structure in Figure 7 (b).

The exchanging orders for the rearranged structure are created from a changed triangular transporter based PWM pulse design as appeared in Figure 8 (a), which is likewise known to enhance the symphonious contortion of the yield voltage.

The bearer recurrence ought to be chosen for the best consonant execution, which may cover the IEEE 519 harmonic standard and channel less operation. The adjustment record is standardized to half of the dc interface voltage U, and the tweak plot satisfies two fundamental necessities:

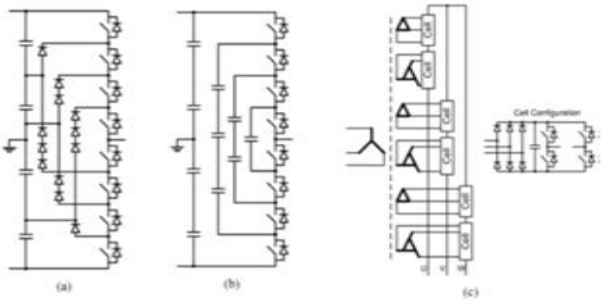
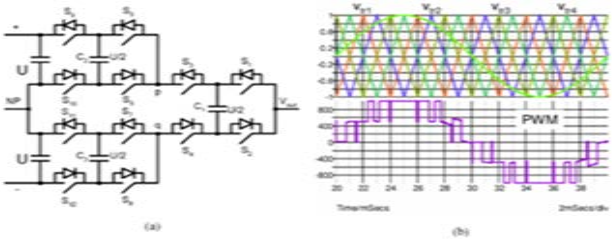
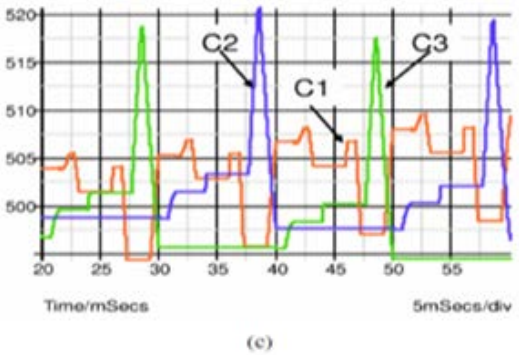


Fig 5(a) NPC, (b) coasting capacitor, and (c) fell H-extension and basic cell.





(c)

Fig 6: (a) ANPC5L multilevel converter, (b) carrier-based PWM and normalized phase voltage, and (c) normalized voltage across the floating capacitors.

All these three signs are utilized for choosing which changing state out of the eight conceivable states ought to be utilized. All switching states and their effect on the coasting capacitor voltage are appeared in Table-II. The yield voltage assumes one of the five voltage levels concerning the impartial point: –U/2, - U/4, 0, U/4, and U/2, which are numbered from0 to 4, individually.

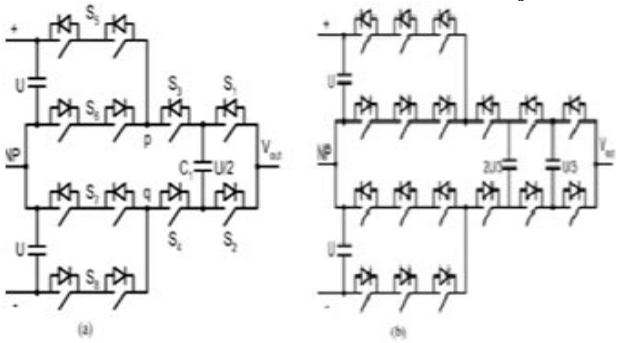


Fig 7: (a) Improved ANPC5L and (b) ANPC7L.

With these level numbers and the three signs specified over, the exchanging states are chosen by fig.5. The indication of the heap current sign (Ix) and the indication of the coasting capacitor voltage deviation sign(Dx) are utilized to choose whether to charge or release CfX utilizing the exchanging states V2 or V3 (Vout < 0), andV6 or V7 (Vout > 0).

TABLE-II: SWITCHING STATES AND IMPACT ON THE FLOATING CAPACITOR VOLTAGE.

Cell 3				Cell 2		Cell 1		Cell Voltages	Phase Voltages	Effects on C_f		Switching state
S8	S7	S6	S5	S4	S3	S2	S1			I >0	I <0	
1	0	1	0	1	0	1	0	-U	-U	-	-	V1
1	0	1	0	1	0	0	1	-U+U/2	-U/2	Discharge	Charge	V2
1	0	1	0	0	1	1	0	-U/2	-U/2	Charge	Discharge	V3
1	0	1	0	0	1	0	1	0	0	-	-	V4
0	1	0	1	1	0	1	0	0	0	-	-	V5
0	1	0	1	1	0	0	1	U/2	U/2	Discharge	Charge	V6
0	1	0	1	0	1	1	0	U-U/2	U/2	Charge	Discharge	V7
0	1	0	1	0	1	0	1	U	U	-	-	V8

utilizing the indication of the reference voltage sign (Vref X), the zero-voltage exchanging state V4 or V5 is selected so that the exchanging recurrence of the "external" and "bracing" switches (S5, S6, S7, S8) brings about the fundamental yield recurrence I {R, S, T}; i.e.: no impact of this variable on the choice of the exchanging state.

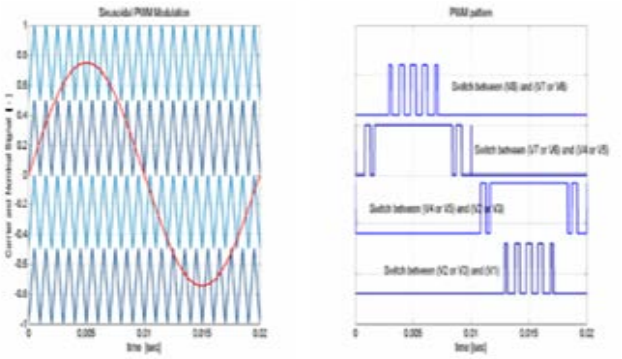


Fig 8: a) Modified carrier-based PWM and b) switching state transitions.

Albeit expanding the quantity of levels enhance the power nature of the yield voltage, more levels may be economically confined by the measure of skimming capacitor that is required bythe converter. The capacitance needed to constrain the voltage swell over the gliding capacitor for a given transporter recurrence can be figured as takes after:

$$C_f = \frac{I_{pk}}{\square v_f} \frac{1}{f_c}$$

Where Ipk is the pinnacle stage current, Vf is the crest to-top voltage swell over the skimming capacitors, and fc is the carrier recurrence.

5. MATLAB SIMULATION RESULTS

To verify the operation of the proposed topology and the performance of the modulation techniques provided in this paper.Aproposed model is developed and simulated with MATLAB SIMULATION software, and compared to the existing system.

5.1 Existing system results:

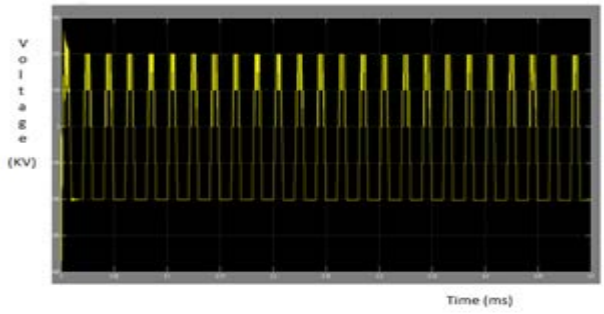


Fig 5.1.1. Phase voltage.

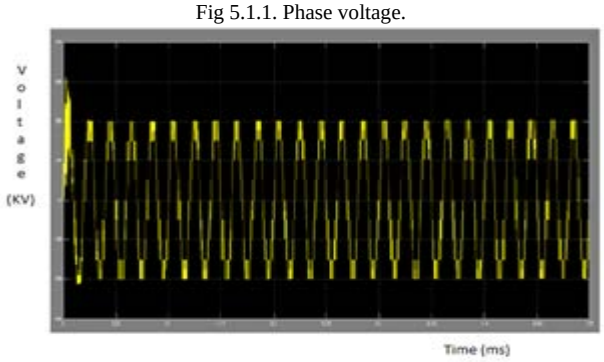
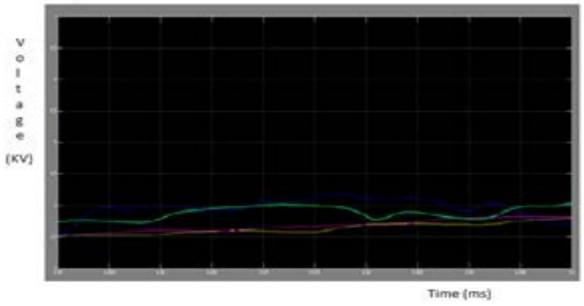


Fig 5.1.2. Line voltage



5.1.3. Flying capacitor voltage

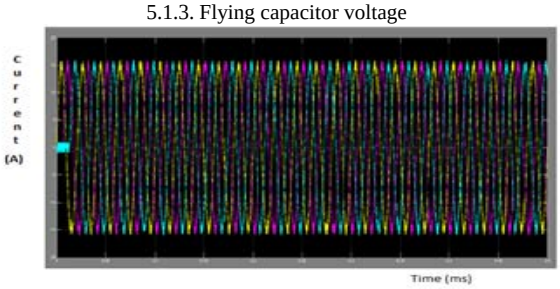


Fig 5.1.4. Load current

Phase Voltage	Level Number	Sign (ΔV_{cfx})	Sign (i_x)	Sign (V_{refx})	Switching state
-U	0	n.e.	n.e.	n.e.	V1
-U/2	1	-1	-1	n.e.	V2
-U/2	1	-1	+1	n.e.	V3
-U/2	1	+1	-1	n.e.	V3
-U/2	1	+1	+1	n.e.	V2
0	2	n.e.	n.e.	-1	V4
0	2	n.e.	n.e.	+1	V5
U/2	3	-1	-1	n.e.	V6
U/2	3	-1	+1	n.e.	V7
U/2	3	+1	-1	n.e.	V7
U/2	3	+1	+1	n.e.	V6
U	4	n.e.	n.e.	n.e.	V8

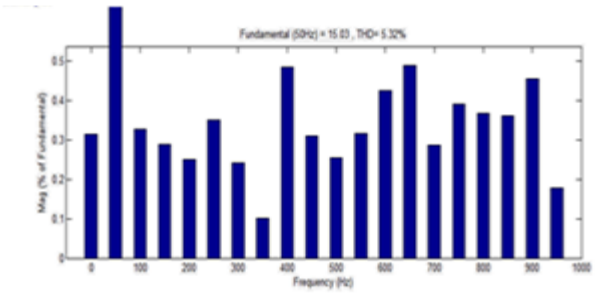


Fig 5.1.5. THD of current.

5.2 Proposed system results:

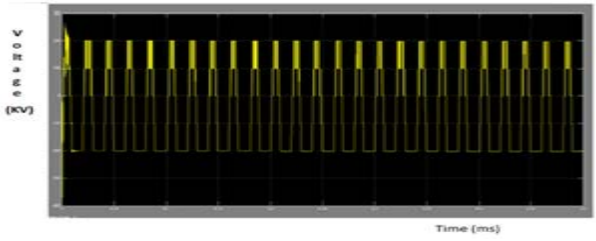


Fig 5.2.1. Phase voltage.

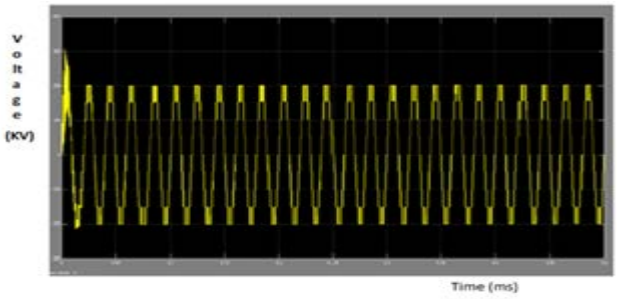


Fig 5.2.2. Line voltage.

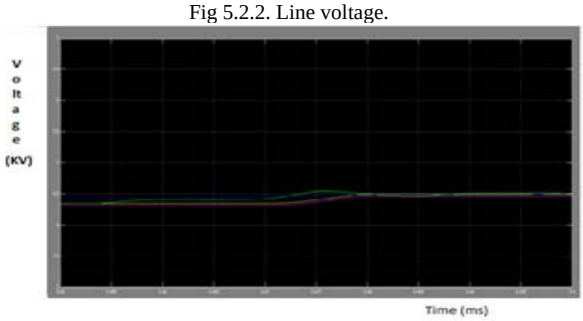


Fig 5.2.3. Flying capacitor voltage.

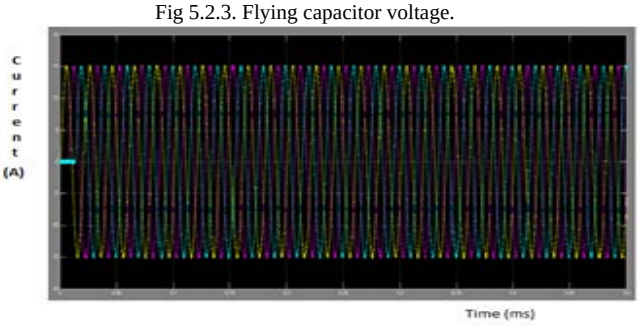


Fig 5.2.4. Load current.

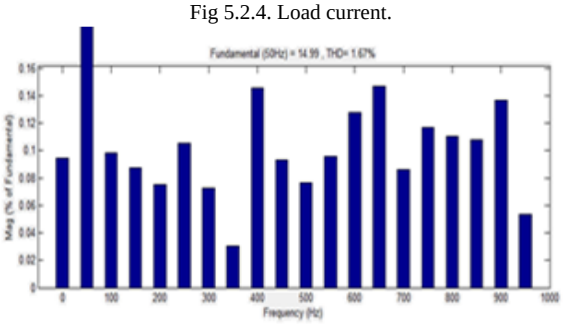


Fig 5.2.5. THD of current.

6. CONCLUSION

In this endeavor, the execution of the five level FC based ANPC converter is proposed. Another mixture of 5-level inverter topology and adjustment strategy is proposed. Contrasted with 5-level ANPC as the most comparable topology, this new topology requires two less switches at the cost of an extra capacitor and six diodes. However, since the capacitors still observe the exchanging recurrence and their size continue as before, it is relied upon to lessen the inverter's aggregate cost. In the same way, dissimilar to 5-level ANPC, all switches must withstand a similar voltage which disposes of the requirement for arrangement association of switches and related synchronous turn on and off issue. Great misfortune appropriation among switches can build the inverters appraised influence or give higher exchanging recurrence and smaller capacitor estimate.

7. FUTURE SCOPE

The converter used in this project can be modified and can be used in the applications of grid connected such that the centralized system can be easily controlled and high amount of power can be produced and with the efficient controllers, the system will be harmonic free.

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