REDUCED LEAKAGE CURRENT USING DOMINO TECHNIQUES

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Abstract— *As the aspect ratio of the devices shrinks down, the power supply voltage should be shortened to meet low power requirements, and the threshold voltage should also be reduced to achieve high performance. This however leads to aggressive increase in leakage current; hence the circuit's reliability is also affected. A new domino circuit is suggested with reduced power and lower leakage for wide fan-in gates. The main intention was to make domino circuits more potent and with lower leakage and without dramatic speed degradation. The technique employed in this paper is that, the pull-up network's mirrored current is compared with its worst case leakage current and it downturns the upper and lower boundary of the voltage swing on the dynamic node. The parasitic capacitance on the dynamic node and the keeper size for very large fan-in gates is also decreased by the expected circuit and hence the circuit can be used as a small keeper for wide fan-in gates to implement fast and robust circuits. The footer transistor is also used to shorten the leakage current. Simulation results of wide fan-in gates are build using Tanner in 16-nm technology.*

Keywords— Domino logic; ;Leakage-tolerant; Voltage Swing; Wide fan-in

1. INTRODUCTION

DYNAMIC gates are used for designing wide high-speed OR and AND gates in CMOS. These gates are especially used in multiport memories for low-power utilization [9]. Domino circuits are used for implementing high fan-in circuits and are broadly used in high-speed operations [6]. With technology scaling, the supply voltage is decreased to reduce the power consumption and the threshold voltage is also shortened to achieve high performance. However, the threshold voltage scaling results in considerable increase of the sub threshold leakage current.

Hence the leakage current [11] must be reduced to obtain sturdy and high performance designs, especially for wide fan-in dynamic gates [3] which have many applications in digital signal processors and high speed demanding units of microprocessors. However, in wide fan-in OR gate, with increasing leakage current, the robustness and performance significantly downgrades. As a result it is difficult to obtain adequate robustness and performance. In this paper, a Current Comparison based Domino (CCD) [8] circuit for wide fan-in applications is discussed which together boosts the performance and shortens the power consumption.

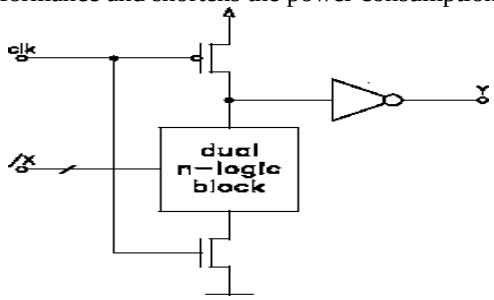


Fig.1 Application of an OR gate using both static CMOS and NMOS domino logic.

Fig.1 shows the application of an OR gate using both static CMOS and NMOS domino logic. In this circuit to establish the robustness of the dynamic nodes a full keeper is added. The keeper ratio is defined as

$$K = \frac{\mu_p \left(\frac{W}{L}\right) Keeper - transistor}{\mu_n \left(\frac{W}{L}\right) evaluation - network} \qquad (1)$$

Where L and W denote the transistor size and μ_n *and* μ_p be the electron and hole motilities respectively.

The robustness of domino circuits can be improved by increasing the size of the keeper transistor. However, this leads to the increase in delay of the circuit, power utilization, degeneration of performance and also rise in the contention current between evaluation network and keeper transistor. As a large number of leaky nMOS transistors are connected to the dynamic node in wide fan-in dynamic gates the above mentioned issues becomes more critical.

Hence there arises a comparison between robustness and performance.

A number of circuit techniques have been proposed in the literature to address these issues such as a Conditional-Keeper Domino (CKD), High-Speed Domino (HSD), Leakage Current Replica (LCR) keeper domino, and Controlled Keeper by Current-Comparison Domino (CKCCD).

2. PROPOSED CIRCUIT

In wide fan-in gates the dynamic node's capacitance is large. So the speed is reduced desperately. Varying the size (increasing) of the keeper transistor results in increased power consumption and delay that is due to increase in contention current. By using the comparison stage [7] the above issues can be dealt up by making the PDN to implement the logical function and separating it from the

keeper transistor. In this stage, pull-up network's current is correlated with its worst case leakage current.

This concept is illustrated in Fig. 2, where the PUN is used rather than PDN. However, there is a match between the reference current and the PUN. When the output node voltage is discarded to ground voltage, the transistor M_k and the reference current are combined in series to reduce power consumption.

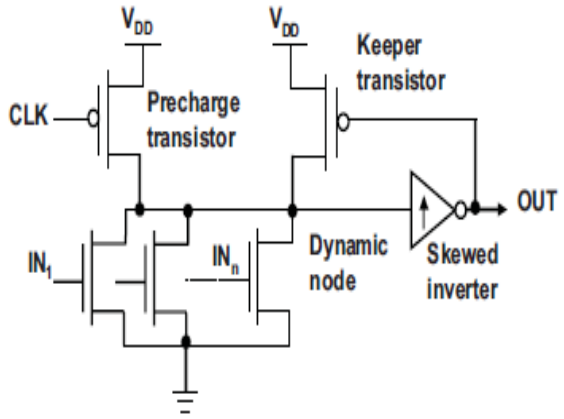


Fig.2. Current Comparison Domino (CCD)

In order to maintain the robustness of the circuit, the reference voltage must be developed according to the correct variation of the reference current and process variations [1]. Process variations appear primarily due to systematic and random parameter variations [2]. In random deviations the parameters of each device vary individually and it is independent of neighboring devices. However in systematic variations the specifications of neighborhood transistors are affected which leads to a heavy interaction between parameters of adjacent devices. Systematic variations are considered in this paper. We have assumed that the threshold voltage of all nMOS and pMOS transistors differs together in a given circuit design. The speed of the circuit and power consumption [4] is straightly affected due to any threshold variations on the voltage at node A and B. Hence these issues are deliberately considered in the proposed circuit.

The worst case is that the threshold voltage of the pMOS is raised and the threshold voltage of the nMOS transistor is reduced i.e. due to process variations [2] it is slow pMOS and fast nMOS. In the previous case, the pMOS transistor's subthreshold leakage in PUN is reduced; hence the reference current must be decreased and same for the recent case also. Therefore, in order to maintain the robustness of the design the reference current must be adjusted according to the variations in the threshold voltage.

The proposed circuit is shown in Fig. 3. The circuit in Fig. 3 is a replica of the PUN's lowest case leakage current and perfectly followed leakage current variations that is due to process deviations. Therefore, the transistorM_7's gate is connected toV_{DD}. As shown in Fig. 3, in the proposed circuit, transistor M_2 is used to mirror the current of the PUN with the reference current, which resembles the leakage current of the PUN.

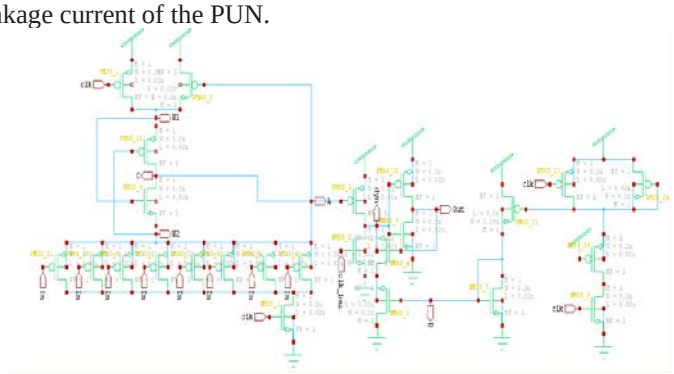


Fig .3 Implementation of wide OR gate (8-input)

In the proposed circuit, nMOS transistors are used to implement the logic function, as shown in Fig. 3. The source and body terminals of the nMOS transistors are linked together in order to eliminate the body effect. So, the threshold voltage of the transistors is only varied and not the body effect due to process variations. By utilizing nMOS transistors in N-well process, the threshold voltage is reduced due to body effect, yielding a decrease in delay.

In other words, nMOS transistors can be used in P-well process to obtain a high speed due to higher mobility of nMOS. Although, the pMOS has lower mobility which reduces the speed, by reducing the capacitance on the dynamic node, the speed can be increased in the proposed circuit by properly choosing the mirror ratio M.

The proposed circuit as shown in Fig. 3 has five additional transistors and a reference circuit that is shared when compared to Leakage Current Replica Keeper (LCR) [5]. The transistorM_7's drain-source voltage is equal to the drain-source voltage of the pMOS transistors in PUN and all have the sameV_{DS}. The transistorM_3's gate leakage is negligible when compared to the mirrored sub-threshold current of the transistorM_7.

The proposed circuit operates in two stages. Pre-evaluation network is the first stage which includes the transistorsM_{Pre}, M_{Eval} and the PUN. The PUN, which implements the logic function, is separated from the dynamic node (DYN), which changes the dynamic voltage indirectly. The second stage resemble like a footless domino which has one input (i.e. node A input as in Fig. 3) that has no charge sharing with the transistor M_2 in spite of the Boolean function implemented by the PUN, and a controlled keeper that contains two transistors. To reduce the capacitance on the dynamic node, a pull-up transistor is connected to the DYN (dynamic node), yielding increase in speed. The first stage prepares the input signal for the second stage.

In the evaluation phase, there are two parts in dynamic power consumption, each for each stage. The dynamic power consumption is directly related to the voltage swing, capacitance, power supply, contention current and temperature. The first stage has no contention current and a

low voltage swing from V_{DD} *to* V_{THP}. There is a rail-to-rail voltage swing at the second stage with minimum contention.

The proposed circuit has less dynamic power consumption even though it has some area overhead. In the proposed circuit, nMOS and pMOS transistors are used below the PUN and PDN respectively [14], to reduce and increase the upper and lower boundary of the voltage fluctuation at the dynamic node.

If the input to the OR gate is low, and if there is at least one conductive path exists between ground and node A, the voltage drop is raised up, which turns on the transistor M_2 and the output voltage is also changed.

Due to the unequal voltage of the body and source terminals, the body effect is not eliminated. If there is a higher deviation that is due to process variation the leakage current will be decreased further.

In the pre discharge mode, the dynamic node is charged to power supply voltage that was at nonzero voltage at the starting. It results in the reduction of power consumption even when the dynamic node's capacitance is large in wide fan-in gates particularly for wide fan-in OR gates. Increasing the size of the transistor M_2 in turn increases the speed.

The mirror ratio M is defined as the ratio of the size of transistor M_2 to the size of transistor M_1.

$$M = \frac{\left(\frac{W}{L}\right) M_2}{\left(\frac{W}{L}\right) M_1} \qquad (2)$$

The proposed circuit as shown in Fig. 4 operates in two phases as follows.

A. Pre discharge Phase

In this phase, the clock voltage is at low level and the input signals are at high level [clk ="0", clk_bar ="1" as in Fig. 3].The transistor M_{Dis} causes the voltages at the node A and the dynamic node to fall to a low level and its raised to a high level by transistor M_{Pre}. Hence the transistors M_2 and $M_{Eval}$are off and the transistorsM_{Pre}, M_{Dis}, M_{k1}, and M_{k2} are on. The output inverter causes the output voltage to rise to a high level.

B. Evaluation Phase

In this phase, the input signals are at low level and the clock voltage is at high level level [clk ="1", clk_bar ="0" as in Fig. 3]. Hence the transistors$\boldsymbol{M_2}$, $\boldsymbol{M_{k2}}$, and $\boldsymbol{M_{Eval}}$ are on and the transistors $\boldsymbol{M_{Pre}}$ and $\boldsymbol{M_{Dis}}$ are off. Depending upon the input voltages the transistor $\boldsymbol{M_{k1}}$ can be on or off. Two stages occurs in this phase. All the inputs may remain high in first stage. Second, all the inputs may remain at the low level. At the first stage, the transistor $\boldsymbol{M_2}$ mirrors the leakage current, which is compensated by the keeper transistors ($\boldsymbol{M_{k1}}$, and $\boldsymbol{M_{k2}}$) at the second stage.

The voltage at node A is decreased to nonzero voltage and the pull-up current is raised, when there is at least one conductive path exists in the second stage. The Mirrored current in transistor M_2 is raised by increasing the pull-up current. Hence the dynamic node's voltage is charged to Vdd. The voltage at the output node is discharged and the main keeper transistor M_{k1} is turned off. The simulated waveforms of the proposed circuit for 8-input OR gate is shown in Fig. 4. The results are obtained using 16-nm technology in TANNER software.

3. SIMULATION RESULTS AND COMPARISONS

The proposed circuit is designed using 16-nm technology in TANNER. 0.8V is used as the supply voltage and the wide fan-in (8, 16, 32, 64 input) OR gate circuit is used as a benchmark. The clock frequency used is 1-Ghz.

The output capacitance load is set as 5 fF heavy load due to the high fan-out. Fig. 4 shows the simulations result of an 8-input AND gate using the proposed circuit

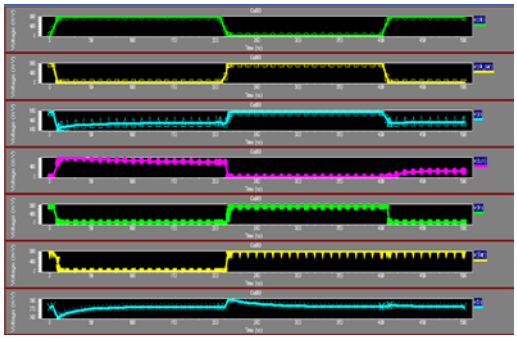


Fig.4 Simulated waveforms of 8-input OR gate using the proposed circuit.

When all the inputs are at high level, the proposed circuit has lower leakage and it meets the high robustness required for wide fan-in gates. The overall leakage current of the proposed circuit is reduced to the source voltage of the PUN transistors. Fig .5 and Fig .6 shows that the power and the Leakage current is reduced in the proposed circuit. Subthreshold current is the major factor of the leakage current and is given by,

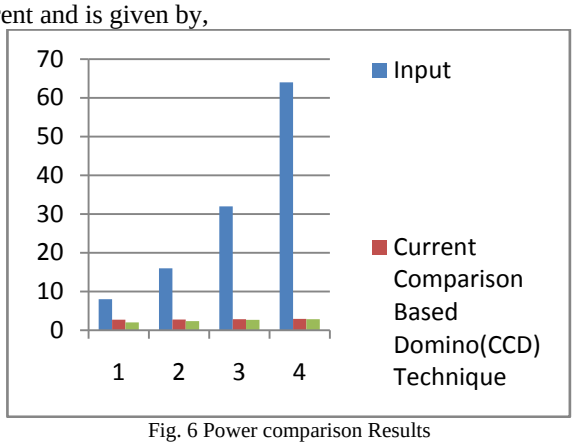
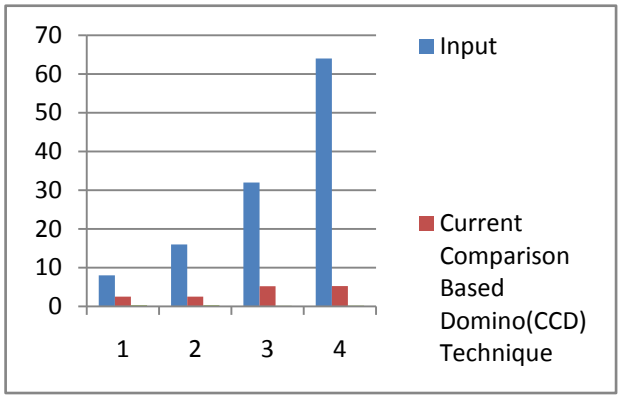


Fig. 6 Power comparison Results



$$I_{Sub\_th} = I_0\left(1 - e^{\frac{-V_{DS}}{V_t}}\right)e^{\left(\frac{V_{GS}-V_{TH}+\eta V_{DS}}{nV_t}\right)} \quad (3)$$

With

$$I_0 = \mu_0 C_{OX}\frac{W}{t}(n-1)V_t^2 \quad (4)$$

where V_{GS} is the transistor gate-source voltage, V_{DS} is the transistor drain-source voltage, V_{TH} is the threshold voltage, $V_t = kT/q$ is the thermal voltage, η is the DIBL coefficient, n is the sub threshold swing coefficient of the transistor, μ_0 is the zero bias mobility, C_{OX} is the gate oxide capacitance, W and L are the width and length of the transistor. In the evaluation phase of the proposed circuit, when all the inputs are at high level, due to the leakage current the voltage at node A is decreased. The PUN transistors V_{SG} will be negative, and according to the above equations we get a lower subthreshold leakage current.

4. Conclusion

With the technology scaling, the leakage current is increased dramatically in wide fan-in gates, resulting in increased power consumption and reduced noise immunity. The worst-case delay can be decreased by increasing the fan-in gates, which in turn reduces the contention current between the evaluation network and keeper transistor. Simulation results show that the proposed circuit has lower leakage and reduced power consumption.

Thus, the proposed circuit can be used for implementing Boolean Logic functions for wide fan-in gates with reduced power and lower leakage.

References

[1] Alioto, M Palumbo, G. & Pennisi, M (2010) "Understanding the effect of process variations on the delay of static and domino logic," IEEE Trans. Very Large Scale (VLSI) Syst., vol. 18, no. 5, pp. 697–710.

[2] Bowman. K, Duval. S. G, and Meindl . J. D (Feb. 2002) "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," *IEEE J. Solid-State Circuits*,vol. 37, no. 2, pp. 183–190.

[3] Dadgour. H. F and Banerjee. K (Nov. 2010) "A novel variation-tolerant keeper architecture for high-performance low-power wide fan-in dynamic or gates," IEEE Trans. Very Large Scale (VLSI) Syst., vol. 18, no. 11, pp. 1567–1577.

[4] Kim, CH. K. Roy, Hsu, S. Krishnamurthy, v & Borkar, v (2006) "A process variation compensating technique with an on-die leakage current sensor for nanometre scale dynamic circuits," IEEE Trans. Very Large Scale (VLSI) Syst., vol. 14, no. 6, pp. 646–64.

[5] Lih, Y. Tzartzanis, N. & Walker, WW. (2007) "A leakage current replica keeper for dynamic circuits," IEEE J. Solid-State Circuits, vol. 42, no. 1, pp.48-55.

[6] Mustafa, V. Anis, M. & Elmasry, M. (2011) "Novel timing yield improvement circuits for high-performance low-power wide fan-in dynamic OR gates,"IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 10, pp. 1785–1797.

[7] Peiravi. A and Asyaei. M (2012) "Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates, integration," VLSI J., vol. 45, no. 1, pp. 22–32.

[8] Peiravi. A and Asyaei. M (May 2013) "Current-Comparison-Based Domino: New Low-Leakage High-Speed Domino Circuit for Wide Fan-In Gates," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, NO. 5.

[9] Rabaey. J. M, Chandrakasan . A, and Nicolic. B, Digital Integrated Circuits: A Design Perspective, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2003.

[10] Roy, K. Mukhopadhyay, S. & Mahmoodi-Meimand, H. (2003) "Leakage current mechanisms and leakage reduction techniques in deepsubmicrometer CMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327.

[11] Shan hag, N. Soumyanath, K. & Martin, S. (2000) "Reliable low-power design in the presence of deep submicron noise," in Proc. ISLPED, pp. 295-302.

[12] Tarun Kumar Gupta, Kavita Khare (February 8, 2013) "A New Technique for Leakage Reduction in 65 nm Footerless Domino Circuits," *Circuits and Systems*, 4, 209-216.

[13] Volkan Kursun and Eby G. Friedman (Apr. 2002) "Low Swing Dual Threshold Voltage Domino Logic,"ACM/SIGDA Great Lakes Symposium on VLSI; pp. 47-52.

[14] Wang. L, Krishnamurthy. R, Soumyanath. K and Shanbhag. N (2000) "An energy-efficient leakage-tolerant dynamic circuit technique," in Proc. Int.ASIC/SoC Conf., pp. 221–225.