

SIMULATION OF ZVS CUK CONVERTER USING PSIM

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*Abstract***—***A Zero Voltage Switching (ZVS)Cuk converter is presented in this paper to reducethe switching losses of main switch. An auxiliaryswitch and a clamp capacitor are connected inparallel with the main switch to absorb all theenergy stored in the leakage* inductance of thetransformer. The ZVS operation of main switch isachieved by the resonance with the resonantinductor and output *capacitor of main switch. TheZVS operation of auxiliary switch is achieved bythe resonance with the resonant inductor and theclamp capacitor. Therefore, both switches areturned on at ZVS. The principle of operation,system analysis and design consideration arepresented. Finally, simulations based on an 270W(18V/15A) are provided for the proposedconverter.*

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Keywords— Zero Voltage switching (ZVS) Cukconverter; Active clamp technique; Soft switching

1. **INTRODUCTION**

Switching mode power supplies are widely used in the personal computer, LCD monitor, charger and telecommunication applications. However, the converters with hard switching techniques result in low efficiency and high voltage and current stresses on the power semiconductors. Soft switching techniques for power converters have been proposed to improve circuit efficiency, increase power density and reduce voltage and current stresses on the switching devices. The asymmetrical PWM techniques [1-3] were proposed to achieve ZVS turn on and to increase circuit efficiency. The drawback of the asymmetrical converter is that the voltage and current stresses of switching devices are related to duty cycle. The full-bridge converters with phase-shift pulse width modulation (PWM) technique [4-5] have been proposed to regulate the output dc voltage and to achieve ZVS operation of power switches. However, the high cost and narrow ZVS range for the lagging leg of the phaseshift full-bridge converter are the main disadvantages. Resonant converters [6- 7] based on the resonant inductor and the resonant capacitor have been proposed to achieve zero voltage switching (ZVS) turn-on or zero current switching (ZCS) turnoff. However, the voltage stress on the power semiconductor is the main drawback in the resonant converters especially for the high input dc voltage.

Higher voltage or current stresses increases the conduction losses compared to the hard-switching techniques. The active clamp techniques [8-11] based on auxiliary switch and clamp capacitor were proposed to reduce the voltage stress of main switch and to increase efficiency of the converter. The active clamp converter uses the transformer leakage inductance and output capacitance of main switch to achieve resonance and to absorb the surge energy stored in the transformer leakage inductance such that the ringing voltage at the transformer primary side is suppressed. The system analysis, circuit design consideration and implementation of a ZVS Cuk converter are presented. The active clamp topology is used in the ZVS Cuk converter to reduce the switching losses on

the power switches and to limit the peak voltage stress on the switches. The soft switching of switches is achieved by the utilization of transformer leakage inductance. The adopted active clamp circuit is connected in parallel with main switch in order to recycle the energy stored in the transformer leakage inductance. The operational principle, analysis and design consideration of the proposed converter are discussed and analysed. Finally, the simulation results are presented to demonstrate the circuit performance. The proposed converter is used in arc welding equipment, motor drive control and in telecommunication applications.

2. ZERO VOLTAGE SWITCHING CUK CONVERTER

A. Design

Fig.1 shows the proposed design of the ZVS Cuk converter. L1, L2, S1 and S2 are input inductor, output inductor, main switch and auxiliary switch respectively. The capacitors C1 and C2 are medium for transferring energy from the source to the load. Cr, Cc,C0, Lm and Lr are resonant capacitor, clamp capacitor, output capacitor, magnetizing inductor of the isolation transformer and resonant inductor respectively. D is the freewheeling diode. Active clamp circuit based on the auxiliary switch S2 and the clamp capacitor Ccachieves ZVS operation and limits the peak voltage stress of main switch S1. In the proposed converter, main switch S1 and auxiliary switch S2 are all turned on at ZVS turn on.

B. Principle of Operation

The Fig.2 shows the key waveforms of the proposed converter. There are five operating stages of the proposed converter in a switching period. Fig.3 gives the equivalent circuit.

In this First stage, main switch S1 is turned on and auxiliary switch S2 is turned off. The input current charges inductor L1. The input currentiL1 increases linearly. The capacitor voltage $V_{cr} = V_{sl,ds} = 0$. The magnetizing inductor voltage $V_{Lm} = V_{c1}L_m/(L_m+L_r) = V_{c1}$. The magnetizing current i_{Lm} decreases linearly. The main switch current is given by $i_{s1}=i_{L1}+i_{L1}=i_{L1}+i_{C1}$. The secondary winding voltage

of transformer Vs=Vc1/n. The diode D is turned off. The inductor current $i_{L2}=i_{C2}$ and increases linearly. The positive current i_{C2} discharges capacitor C2. This stage ends at time $t=t2$ when the main switch S1 is turned off and the input inductor current reaches the maximum value.

In the second Stage, at time $t=t/2$, main switch S1turns off. The input inductor current iL1 and capacitor current ic1 charge capacitor Cr from 0 to Vcc. The primary side voltage V_{Lm} =(VCr-Vc1)Lm/(Lm+Lr)= Vcr-Vc1. The diode current at the secondary side iD=0. At time $t=13$, the resonant capacitor voltage Vcr=Vcc, and the primary side voltage VLm »VCc-VC1=nVc2. The diode D turns on at time $t=t3$.

In the third Stage, at time t=t3, the anti-parallel diode of auxiliary switch S2 turns on and the diode Dat the secondary side turns on. The secondary side voltage Vs =- VC2. Before the current iCc is negative, the auxiliary switch S2 should be turned on to achieve ZVS operation. The input inductor current iL1decreases linearly. The voltage across the primary side VLm=nVc2. The capacitor voltage Vc1 is assumed to be a constant value in this stage. The resonant components in this stage include Lr and Cc. Before the clamp capacitor current iCc becomes negative value, the auxiliary switch S2 turns on at ZVS. The diode current iD $=i0-iC2$. The clamp capacitor current iCc will change sign from positive to negative. When the current iCc becomes negative, the clamp capacitor Cc begins to discharge. The capacitor voltage Vcr equals clamp capacitor voltage Vcc. The input and output inductor currents iL1 and iL2 decrease linearly. This operating stage ends when auxiliary switch S2 turns off.

In the fourth stage, auxiliary switch S2turns off. The capacitor current iC1 is positive and greater than input inductor current iL1 so that the switch current is1 is negative and discharge resonant capacitor Cr. The primary side voltage VLm=nVC2 and the magnetizing inductor current increases linearly. The negative switch current is1 discharges capacitor Cr from Vcc to 0 in this stage. To ensure ZVS operation of main switch S1, the capacitor voltage Vcr should reach zero before the end of this stage. Therefore the energy stored in the resonant inductor Lr must be greater than the energy stored in the resonant capacitor Cr. At time t=t5, the resonant capacitor voltage Vcr=0. The diode D at the secondary side is in the freewheeling mode. This time interval is very short. Therefore the primary side and secondary side currents are almost constant.

In the fifth stage, at time $t=15$, the resonant capacitor voltage Vcr=0 and the anti-parallel diode of main switch S1 turns on. The secondary side diode is still in the freewheeling mode. The input inductor current, primary current and main switch current increase linearly. Before the switch current is1becomes positive, the main switch S1 should be turned on to achieve ZVS operation. The secondary side diode current ID decreases until to zero. At this moment the stage 5 ends and the circuit goes to the operating stage 1. This stage ends at $t=t1$ when diode current ID is decreasing to zero.

3. ANALYSIS AND DESIGN

In the system analysis of the ZVS Cuk converter, the following assumptions are made:(1) $Cc \gg Cr$; (2)Lr<<Lm; (3) All semiconductor components are modeled as ideal; (4) The turn ratio between the primary winding turn of transformer and the secondary winding turn is $p \, s \, n = n / n$; and (5) The energy stored in the resonant inductance Lris greater than energy stored in the resonant capacitance Cr to achieve ZVS operation. In this analysis, the voltage second product across the input inductor when main switch and body diode are turned on equals the voltage-second product when both main switch and body diode are turned off.

$$
V_{in} \ DT_s = (V_{cc} - V_{in})(1 - D)T_s
$$

Where D is the duty cycle of main switch S1 and Vin and Vcc are average voltage value of input voltage and capacitor.

The clamp capacitor voltage Vcc, capacitor voltages Vc1 and Vc2 and output voltage V0 are expressed as:

$$
V_{cc} = \frac{1}{1 - D} V_{in}
$$

\n
$$
V_{c1} = V_{in}
$$

\n
$$
V_o = V_{c2} = \frac{D - D_{loss}}{n(1 - D + D_{loss})} V_{in}
$$

Where Dloss is the duty cycle loss of the proposed converter. When switch S1 is turned on, the current ripple on the magnetizing inductor is given as follow.

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$$
\Delta i_{Lm} = \frac{(D - D_{Loss})T_s V_{c1}}{L_m} V_{in} = \frac{(D - D_{Loss})T_s V_{in}}{L_m}
$$

The ripple currents on the input and outputinductors L1 and L2 are given as:

> $\Delta i_{L1} = \frac{DT_{s}V_{in}}{L_{1}}$ 2 $v_2 = \frac{(1 - D + D_{Loss})I_sV_0}{I}$ $(1 - D + D_{Loss})$ $\Delta i_{L2} = \frac{(1 - D + D_{Loss})T_s V}{L_2}$

If the ripple currents on the input and output inductors are given, the input and output inductance scan be obtained as:

$$
L_1 = \frac{DT_sV_{in}}{\Delta i_{L1}}
$$

$$
L_2 = \frac{(1 - D + D_{Loss})T_sV_0}{\Delta i_{L2}}
$$

The turns ratio between the transformer secondary side and primary side is equal to

$$
n = \frac{(D_{\text{max}} - D_{\text{Loss}})V_{\text{in}}}{(1 - D_{\text{max}} + D_{\text{Loss}})V_{o}}
$$

Where Dmax is the maximum duty cycle when input voltage Vin is minimum. To achieve ZVS operation, the time period is equal to

$$
t_d = \frac{\sqrt{L_r C_r}}{4}
$$

If the resonant capacitance Cr is given, the resonant inductance Lr can be expressed as

$$
Lr = \frac{4t_d^2}{C_r \pi^2}
$$

One half of the resonant period is approximately equal to the turn off time of main switch

$$
\frac{T_r}{2} = \pi \sqrt{L_r C_c} = (1 - D)T
$$

Therefore the clamp capacitance can be obtainedas:

$$
C_c = \frac{\left[(1 - D)T \right]^2}{\pi^2 L_r}
$$

4. SIMULATION RESULTS

Fig.3 shows the simulation circuit of the proposed Converter using PSIM.

Fig. 4 Waveforms of input voltage, input current, outputvoltage and output current.

Fig.4 gives the simulated waveforms of input voltage Vin, input current Iin, output voltage V0 and output current I0.The output voltage of the proposed converter is less sensitive to the load variations. The measured efficiency of the proposed converter is 96% at the rated output power (18V/15A).

5. CONCLUSION

This paper presents the system analysis, circuit design consideration and simulation of a ZVS Cuk converter. The active clamp circuit is used in the proposed converter not only to recycle the energy stored in the transformer leakage inductor but also to increase the circuit efficiency. The mathematical equations of the proposed converter are analyzed. The design consideration of the converter is also included. Finally, the simulation results based on a circuit with 18V/15Aoutput are provided. From the simulation results, the ZVS operations of main and auxiliary switches are achieved.

REFERENCES

- [1] B.Choi, W.Lim, S.Bang, and S.Choi, "Small-Signal Analysisand Control Design of Asymmetrical Half-Bridge DC-DCConverters," IEEE Trans. Ind. Electron., vol. 53, no. 2, pp.511-520, April 2006.
- [2] X.Xu, A.M.Khambadkone, T.M.Leong, and R.Oruganti, "A1- MHz Zero-Voltage Switching Asymmetrical Half-BridgeDC/DC Converter: Analysis and Design," IEEE Trans. PowerElectron., vol. 21, no. 1, pp.105-113, Jan 2006.
- [3] B.Choi, and W.Lim, "Current-mode control to enhanceclosedloop Performance of asymmetrical half-bridge DC-DCconverters", IEEE Proc. – Electric Power Appl, vol. 152, no.2,pp. 416-422, March, 2005.
- [4] B.R.Lin, K.Huang, and D.Wang, "Analysis andimplementation of full bridge converter with current doublerectifier", IEEE Proc. – Electric Power Appl., vol.152, no. 5,pp. 1193-1202, September, 2005.
- [5] J.Yungtack, J.M.M.Jovanovic, and Y.M.Chang, "A new ZVSPWMfull-bridge converter", IEEE Trans. Power Electron.,vol.18, no.5, pp.1122-1129, Septemter, 2003.
- [6] C.A.Canesin, and I.Barbi, "Novel zero-current-switchingPWM converters", IEEE Trans. Ind. Electron., 1997, vol.44,no. 3, pp. 372-381, May 1997.
- [7] G.Hua, and F.C.Lee, "Soft-switching techniques in PWMconverters," IEEE Trans. Ind. Electron., 1995, vol. 42, no. 6,pp. 595-603, November 1995.
- [8] Q.M.Li, and F.C.Lee, "Design consideration of the active lampforward converter with current mode control duringlargesignal transient", IEEE Trans. Power Electron., vol. 18,no. 4, pp. 958-965, July, 2003.
- [9] G.B.Koo, G.W.Moon, and M.J.Youn, "Analysis and design ofphase shift full bridge converter with two seriesconnectedtransformers," IEEE Trans. Power Electron., v ol.19, no. 2,pp. 411- 419, March,2004.
- [10] B.S.Lim, H.J.Kim, W.S.Chung, "A self-driven active clampforward converter using the auxiliary winding of the powertransformer", IEEE Trans. Circuits Syst. II, Analog and Digit.Signal Process., Vol. 51, no. 10, pp. 549-551, Oct. 2004.
- [11] M.Mezaroba, D.C.Martins, and I.Barbi, "A ZVS PWM inverter with active voltage clamping using the reverse recovery energy of the diodes", IEEE Trans. Circuits Syst. I,Fundamental Theory and Applic., vol. 52, no. 10, pp. 2219-2226, Oct. 2005.