SURVEY ON SCHEMES FOR FAULT TOLERANCE OF PARALLEL FILTERS

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Abstract*—Maintaining high reliability in fault detection is a prominent concern in case of life critical missions. Digital filters are widely used in signal processing and communication systems like Electro Cardio Graph Signal Processors and in unmanned space missions. As the complexity of communications and signal processing systems increases, so does the number of blocks or elements that they have. The increase in complexity also poses reliability challenges and creates the need for fault-tolerant implementations. This paper proposes an efficient coding scheme for making the digital FIR filters fault tolerant and to improve the performance of the filters. Fault tolerance requires hardware redundancy and all the existing techniques uses redundant modules for that. In this technique the hardware utilization of the existing technique is minimized. Our proposed model is area efficient as it reduces the number of redundant modules used for error detection and error correction. For any number of filters number of redundant modules would be the least in this system.*

Keywords*—*Algorithm Based Fault Tolerance; Algorithmic Soft Error Tolerance; Single Event Effects; FIR filter

1. INTRODUCTION

The number of transistors integrated per chip and system performance has been improving exponentially, and the complexity of electronic circuits is also increasing day by day. In air, rail, and automotive applications which need crucial reliability, presence of electronic circuits is abundant. Faults that remain after design of the system especially glitches cause system collisions during peak demand resulting in service disruptions and financial losses. Number of transistors in a dense integrated circuit approximately doubles every two years this was stated by the well-known Gordon Moore which was known by Moore's Law. This increased intricacy makes the circuit more vulnerable to errors. Manufacturing variations and soft errors are the major reliability challenges. Undesired outputs are mainly due to soft errors. It is the temporary state or transition which inverses the original state of the system. If any high energy particle hits a circuit node the energy gets transferred to the circuit node, which results in spurious transition and can change the logical value of a circuit node by creating a temporary error that can affect the system operation. Silicon on Insulator (SOI) which is a special manufacturing process was used to protect the circuits. Major breakthrough for protection of the circuits was the ideology to add redundancy.

2. LITERATURE SURVEY

Triple Modular Redundancy (TMR) is the most accustomed technique which makes design three fold the system and adds voting logic to correct errors. It is the best example of a technology which uses the concept of redundancy. Redundant modules are additional systems which are used to protect the desired system. As it triples the area and power of the circuit, it is not acceptable in some applications. Another method [4] is to use the algorithmic properties of the circuit to detect or correct errors which can reduce the overhead required to protect the circuit. This is referred to as Algorithm-Based Fault Tolerance (ABFT). Over the years as the technology has been scaled from about 1300nm to about 10 nm technology, large number of transistors are integrated on a single chip. Complex signal processing applications and biomedical applications use parallel digital filters for the processing of the large number of filters. In this paper most efficient protection scheme with minimal hardware utilization is explored by replacing multipliers with shifters. For many applications signal processing circuits are well suited. These circuits mainly include parallel digital FIR filters. FIR filters are most often chosen over IIR filters as they have regular structures and are stable at linear phase. Over the years, many ABFT techniques [3] have been proposed to protect the basic blocks that are commonly used in those circuits. Parseval theorem [4] was one of the most basic algorithms used to check the error rate in a system. In [5] mitigation of soft errors was the main concern and there various technologies were proposed like self-checking design, Error masking design, error trapping design which was based on Muller C element. Then shim came with the concept of Algorithmic soft error tolerance. Three distinct techniques were proposed [6] and compared their protection efficiency. The Fine Grain Soft Error Tolerance and Sub word Detection processing schemes were explored in [7] which exploits the concept of logic masking. In bridging concurrent and noncurrent error detection multipliers are replaced by constant shifting [8] this idea was explored to make a new scheme for protection .An arbitrary matrix designed [2] to protect the parallel filters with less number of redundant modules was also used in this scheme.

3. VARIOUS SCHEMES FOR FAULT TOLERANCE OF FILTERS

Before going to explore various fault tolerant schemes the concept of fault and its aftereffects should be understood.

Single event effects are the root cause of faults in digital systems.
Single Event effects include Single Event Upsets, Single Event Transients, Single Event Gate Rupture, etc. These faults are all caused due to the undesired current burst occurring in the system. The major technologies considered for fault tolerance were:

A. *Triple Modular Redundancy*

Von Neumann proposed DMR technique, which had been used in early stages of fault tolerant systems [4].

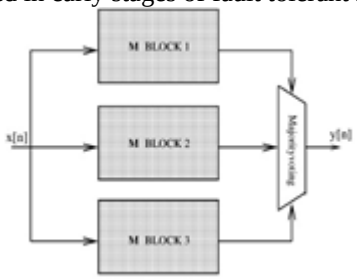

Figure 1: Architecture of TMR

In a TMR system, it consists of 3 modules of the same logic functions which ran in parallel and their output connected to a voter to produce a single output. If any one of the three systems fails, the other two systems can correct and mask the fault. Thus the faulty module could be distinguished by comparing the outputs of the same module and voting for the majority one In fault- tolerant systems by TMR method, it composed of functional block (FB) and a spare block (SB) correspond to each FB, which has same modules and routing as the functional block .If any fault is detected in the FB it is automatically switched to the SB.

Features

- Implements the system three times for protection and back up of the system.
- It was the most accustomed technique for the past Decade.

Disadvantage

- Low fault coverage.
- Large area is utilized for system implementation.

B. *Algorithm Based Fault Tolerance Technique*

The Reddy and P. Banerjee [4] et al. proposed "Algorithm-based fault detection for signal processing applications". Algorithm-based fault tolerance detection is a system level approach that exploits the properties of the architecture and the problem to achieve fault detection/tolerance at a low an error-detection technique called the sum-of squares. This correspondence presents a functional-level concurrent error-detection scheme for such VLSI signal processing architectures proposed for the FFT and QR factorization. Some basic properties

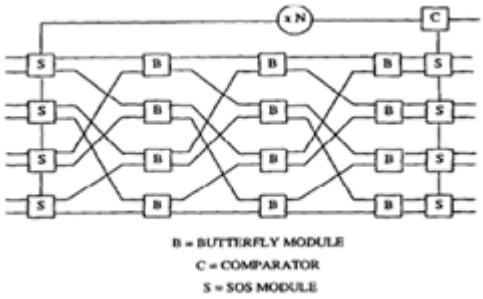

Figure 2: Architecture of ABFT of an FFT

Involved in such computations are used to check the correctness of the computed output values. This fault detection scheme is shown to be applicable to a class of problems rather than a particular problem unlike the earlier algorithm-based error-detection techniques. The effects of round off or truncation errors due to finite-precision arithmetic are evaluated.

Advantage

- Effective with large word lengths.
- Error Detection is possible for algorithm based systems.

Disadvantage

- Low fault coverage.
- Errors are detected, but not corrected

C. *Algorithmic Soft Error Tolerance*

Yuan-Hao Huang [5] investigates the effects of soft errors in the arithmetic circuit and provide an efficient solution for the soft-error-tolerant DSP circuit and described the logic masking property of the soft error in the combinational circuits. This property is utilized to mask the Single Event Upset (SEU) caused by energized particles in the inactive area. To further improve the performance, the masked portion of the datapath can be used as the estimation redundancy in the Algorithmic Soft Error Tolerance (ASET) technique.

Three distinct ASET techniques were proposed they are:

- Spatial ASET
- Temporal ASET
- Spatio Temporal ASET

The soft error in each processing element (fine grain) can be recovered by the arithmetic data path-level ASET technique. Analysis of the fast Fourier transform processor example shows that the proposed FGSET architecture can improve the performance of the Coarse Grain Soft Error Tolerance (CGSET) by 8.5 dBs ASET was proposed to reduce the cost of TMR by using reduced precision modules as the redundancy in the digital signal processing (DSP) system. However, the superior performance may degrade quickly as the soft error rate increases. The implemented Algorithmic soft error tolerant system is shown in fig 3.

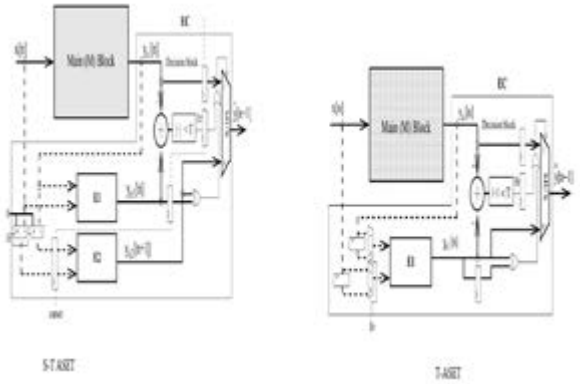

Figure 3 : Spatio-Temporal Algorithmic soft error tolerant system an and temporal Algorithmic soft error tolerance system

Advantages

- Error Detection and Correction possible.
- Area, power & Energy overhead-smaller than Triple Modular Redundancy [TMR].

Disadvantages

- Error Detection is not possible on minute error rates (Per <10-2).

D. Conventional Technique

The protection of parallel filters was done using Error Correction Codes basically Hamming codes. Hamming codes are mainly used to locate whether any transmitted bit is in error and to correct it, so that error free bits are received at the receiver. To protect information bits to be transmitted from errors Hamming codes transmit some number of parity bits along with the information bits. The number of parity bits to be added is based on the Hamming rule.

$$r+p+1 \geq 2p \qquad (3)$$

So according to these observations to protect four information bits from errors three parity bits have to be added. It is explained in Table 1.With the same concept of hamming codes erroneous outputs and faulty filter can be corrected.

TABLE I: REALIZATION OF ERROR CORRECTION CODE BASED SCHEME

S1	S2	S3	Faulty Filter	Action
0	0	0	None	None
1	1	1	F1	Correct F1
1	1	0	F2	Correct F2
1	0	1	F3	Correct F3
0	1	1	F4	Correct F4
1	0	0	F5	Correct F5
0	1	0	F6	Correct F6
0	0	1	F7	Correct F7

Here in the conventional scheme inputs are represented as Xin1, Xin2, Xin3, and Xin4 these are processed through filters with same response arranged in parallel. Considering equation1 and figure2 the responses of the given inputs are Yout1, Yout2, Yout3, and Yout4. For example

$$\text{Yout1}=\sum_{l=0}^{N}(x1 \cdot h[l]) \qquad (4)$$

Inputs to the redundant filters were coded according to the hamming codes and its response is given as

$$\text{Q1 [n]} = \sum_{l=0}^{N}(x1 + x2 + x3)h[l]) \quad (5)$$

Where Q1[n] is the output of the first redundant filter and similarly Q2[n] and Q3[n]. These equations of the output of the redundant filters are taken to check whether there is any error in the output or to find any faulty filter. That is expressed as

$$\text{Q1 [n]} = \text{Y1+Y2+Y3} \qquad (6)$$

Equations 5 and 6 are then equated and checked for equality. Similarly Q2 [n] and Q3[n] are also equated to corresponding sum of outputs. Thus there are three sets of equations which were expressed as

$$\text{Q2 [n]} = \text{Y1+Y2+Y4} \qquad (7)$$

$$\text{Q3 [n]} = \text{Y1+Y3+Y4} \qquad (8)$$

Now these equations 6, 7 and 8 were checked for equality and if all the three were not satisfying the equations then first filter is faulty so as to produce an undesired output. And if 6 and 7 are not satisfied then filter 2 is faulty. Filter 3 is faulty if 6 and 8 are not gratified.

After finding the faulty filter we correct it by reconstructing the outputs. The reconstructed outputs are:

$$Y_{c1}\,[n] = Q1\,[n] - Y2 - Y3. \qquad (9)$$

$$Y_{C2}\,[n] = Q2\,[n] - Y1 - Y4. \qquad (10)$$

$$Y_{C3}\,[n] = Q3\,[n] - Y1 - Y4. \qquad (11)$$

$$Y_{C4}\,[n] = Q2\,[n] - Y1 - Y2. \qquad (12)$$

4. CASE STUDY

Here two types of configurations were selected and a study was conducted on the basis of it. Four parallel digital FIR filters were protected using TMR, spatial ASET, and error correction code basically hamming code based technique. Similarly a configuration of eight parallel filters was also studied.

TABLE III: COMPARISON OF ARE UTILIZATION OF VARIOUS SCHEME FOR FAULT TOLERANCE

System to be Protected	Protection Schemes	Number of Slices	Number of 4 input LUT's	Number of GCLKs	Number of DSP48's
Four Parallel FIR filters	TMR	789	1232	4	29
	S-ASET	674	1179	3	28
	ECC scheme	274	479	2	14
Eight Parallel FIR Filters	TMR	4258	5213	6	37
	S-ASET	3101	4988	5	38
	ECC scheme	1024	1767	3	36

5. CONCLUSIONS

A novel technique to execute fault tolerant parallel FIR digital filters has been proposed in this paper. The anticipated scheme manipulates the linearity of filters to implement an error correction method. Here inputs of two redundant filters which are linear combinations of the original filter inputs are used to detect and locate the

errors. The previously proposed technique was based on the use of Error Correction Codes (ECCs). This method considers each filter as a bit in the ECC. The proposed scheme beats the ECC technique (similar fault-tolerant capability with lower cost). Therefore, the proposed scheme can be useful to implement fault tolerant parallel filters.

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