DESIGN FOR LOW SUPPLY VOLTAGE IN SRAM OF LEAKAGE COMPENSATION

Mohan R[1] | Vinitha K V[2]
[1](ECE, M.P.Nachimuthu M.Jaganathan Engineering College, Erode, India, lakshin204@gmail.com)
[2](ECE, M.P.Nachimuthu M.Jaganathan Engineering College, Erode, India, vinitha.ece7@gmail.com)

***Abstract*—*A leakage current compensation design for nano scale SRAMs is proposed in this paper. The proposed SRAMs cell is implemented with transmission gate. The proposed compensation design is composed of a leakage current sensor and compensation circuit. The leakage current sensor, which generates a warning signal if the leakage is over a predefined threshold, and a compensation circuit following the sensor, which will be activated to speed up the read operation. It is used to enhance the write ability of the SRAM cell using transmission gates and further modification is done in the write assist circuit to reduce the power consumption and delay. The proposed circuit gives better result. The proposed Static Random-Access Memory is implemented using the TSMC 40-nm (CMOS) Complementary Metal Oxide Semiconductor logic technology. The energy per access is measured to be 0.9411 pJ given a 600-mV power supply and a 54-MHz system clock rate. The reduce power delay 2.58ns and 27.86% of the average power dissipation reduced.*

Keywords—Compensation circuit, disturb free, leakage current sensor, single-ended Static Random-Access Memory cell, SRAM

1. INTRODUCTION

SRAM has been an important role in many products, e.g., the cache of CPU. SRAM is faster and more expansive .To extend the operation time and reduce power dissipation, Static Random-Access Memory (SRAM) is usually fabricated using advanced processes. SRAM is a type of semiconductor memory. The on chip memory support circuitry implements read/write functions. Therefore, to reduce the leakage and increase the operation speed, two major design approaches were proposed as follows.

A. Current Mode Sense Amplification

The sense amplifier is one of the most important components of semiconductors memories used to sense stored date. This plays an important role to reduce the overall sensing delay and voltage.

Earlier voltage mode sense amplifier are used to sense the date it sense the voltage difference at bit and bit lines and memory size increase the bit line and date line capacitances increase. Since the CMOS technology has been scaled down very fast, the bitline capacitances may be too large for an SRAM cell to drive.

During a read operation, the sense amplifier predetermines the output result by sensing the differential current on two bitlines (BL_1 and BLb_1), as shown in Fig. 1, such that the low power and high speed would be feasible. Notably, the output delay is irrelevant of the bitline capacitances in such a scenario.

B. Current Compensation Circuit

One of the classic current compensation circuits is shown in Fig. 2. When the SRAM begins to work, the current compensation circuit detects the leakage current of each bitline, and then injects a proper current into the corresponding bitline.

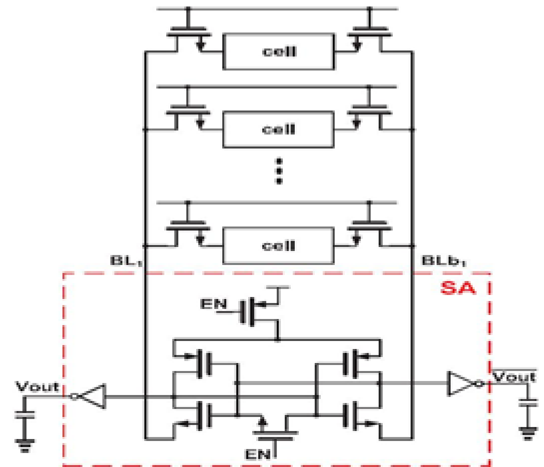

Fig .1curent Mode Sense Amplification

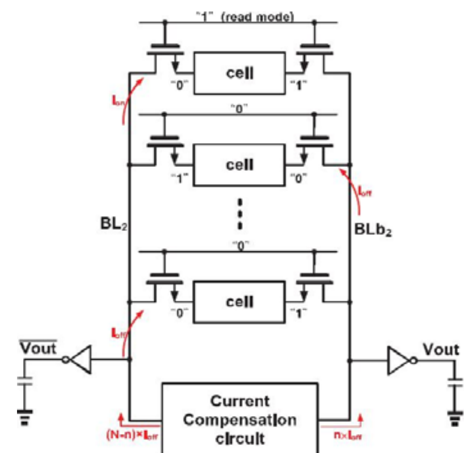

Fig.2 SRAM with Current Compensation Circuit.

The increased leakage current may slowdown the performance of the read operation of SRAM because the existence of the leakage current in the bitline may postpone

the time to resolve the sufficient differential bitline voltage for Sato sense correctly.

For an example, an SRAM array has N cells, where n of the N cell is stored with logic 1, and the rest are stored with logic 0, as shown in Fig. 2. If the bitline leakage is detected, the current compensation circuit injects $n \times I_{OFF}$ into BLb_2, and $(N - n) \times I_{OFF}$ into BL_2, where I_{OFF} is the cutoff leakage current. Then, when one of the SRAM cells is activated to read mode, the speed will be enhanced, since the cell does not need to be affected by the leakage current caused by the other cells. Although this way cannot reduce the leakage current, the access speed of the SRAM will be improved.

1) 5T SRAM

The structure of the Existing SRAM using the leakage current sensor and the compensation circuit is shown in Fig. 3

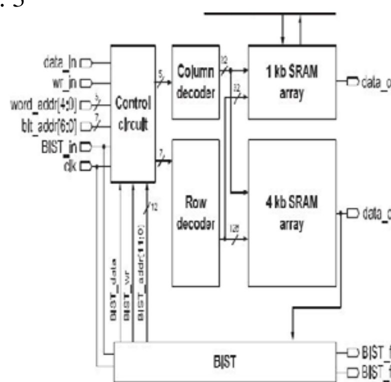

Fig.3 Block Diagram of SRAM.

SRAMs contribute to a significant portion of the total power dissipation. SRAMS usually support read and write operation. The compensation circuitry, two SRAM arrays arrays are carried on the same die sharing common row decoder and column decoder the 1-kb SRAM array with compensation only needs bit_addr, while the 4-kb SRAM array without compensation needs bit_addr. A control circuit includes several MUXs, which allow BIST_in to select either the normal operation mode or the build-in-self-test (BIST) mode. wr_in determines the entire SRAM is the read mode (wr_in = logic 1) or the write mode (wr_in = logic 0), respectively. word_addr and bit_addr drive column and row decoders to select the corresponding cell, respectively. Data will be stored in the SRAM array via data_in. clk represents the system clock. Notably, the output of the compensated design is data_out_t, while the output of the uncompensated design is data_out.

A. *Analytical Models for SRAM Leakage Current*

The objective of this work is to develop models parameterized in terms of high level design parameters. As indicated in Section 3, SRAMs are primarily composed of 6 sub-blocks: memory-core, address decoder, read column circuit, write column circuit, read control and write control circuit. We consider the typical implementation styles of these sub-blocks and develop leakage power models for each sub-block in each of its operational phase (read, write, precharge, and idle). To simplify the analysis, we assume that the leakage current in a sub-block during a transient state is same as the leakage current when it reaches a steady state. Although this approximation might introduce some error, we show in Section 6 that the error margin is reasonable.

B. *Single Ended Disturb Free With 5t SRAM Cell*

Fig.4 shows a 5T SRAM cell coupled with an inverter. Where a load less SRAM cell with write assistant lop and an isolated word line controlled transistors (WLC) is revealed. A shared bitline Inventories included to boost the read access speed at the minimal expense of area cost.

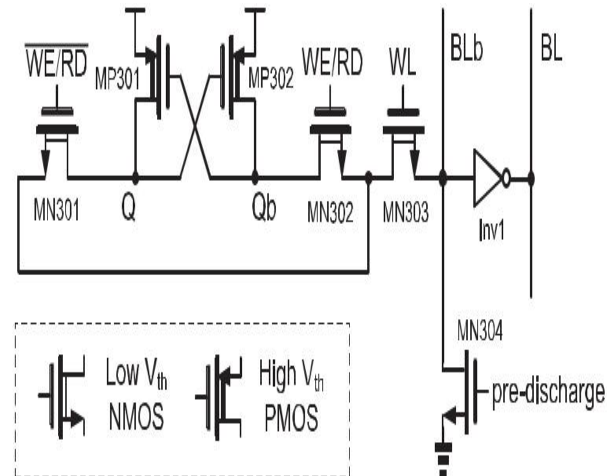

Fig.4 schametic of 5T SRAM Cell.

. To reduce the cutoff leakage current, high V_{th} pMOS transistors, MP301 and MP302, consist of a latch like storage. Low V_{th} nMOS transistors, MN301 and MN302, are used as access switches to supply large current for driving the bitline. The single-ended 5T structure is featured by an additional MOS, MN303, which is controlled by word line (WL) to access Qb such that the internal data state stored in Q will not be interfered by the other cells coupled to BLb. Several advantages of the single-ended disturbfree 5T loadless SRAM cell have been reported, including low power, better read static noise margin (SNM), and disturb free write access.

- Read Operation

The column address decoder select one of word lines. Each column of SRAM cell sends its output to the sense amplifier.

Step 1: Referring to Fig. 5, after clk rises high, the predischarge is then pulled high to discharge BLB to ensure that the parasitic capacitance on BLB would not be charged back to the SRAM cell.

Step 2: After discharging BLB, WL and WE/RD are pulled high to turn ON MN303 and MN302,respectively. Meanwhile, the state of Qb will be coupled to BLB.

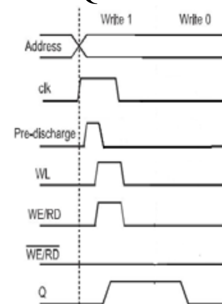

Fig.5 Read Timing Diagram.

- Write Operation

The data is gated to the write drive, which generates input to all therows .the column decoder select the pair of bit lines that are driven.The row decoder enables a row of SRAM cells.

Step 1: Referring to Fig. 6, after clk rises high, the predischarge is pulled high to discharge BLB.

Step 2: If data_in is logic 1 (or 0), WL and WE/RD (or WE/RD) are high to turn ON MN303 and MN302 (or MN301), respectively. Meanwhile, the state of Qb (or Q) will be coupled to BLB, so that it will be overwritten.

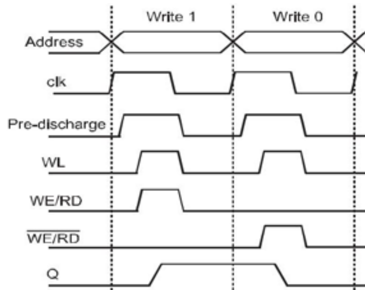

Fig.6 Write Timing Diagram.

2) 5T SRAM WITH TRANSMISSION GATE LEAKAGE SENSOR AND READ DELAY COMPENSATION

A transmission gate is similar to a relay that can conduct in both direction or block by a control signal with almost any voltage potential. It is CMOS based switch in which PMOS passes a strong 1 but por0 and NMOS passes strong 0but poor 1.Both PMOS and NMOS work simultaneously.

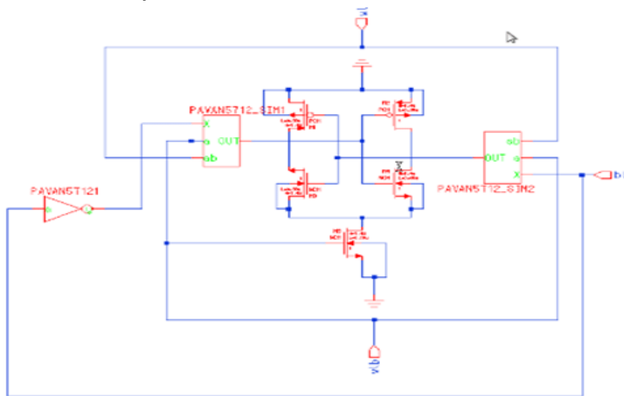

Fig.7 proposed 5T SRAM with transmission gate.

Fig.7 shows the proposed 5T SRAM with transmission gate.The proposed compensation design is composed leakage current sensor and compensation circuit.A novel five transistor SRAM cell presented for application in high speed,low power cache.

It is used to enhance the write ability of the SRAM cell using transmission gates and futher modification is done in the write assist circuit to reduces the power consumption and delay.The proposed circuit gives better result.The 5T SRAM cell is proposed with fast performance and low power consumption.

A. *Leakage Current Sensor and Compensation Circuit.*

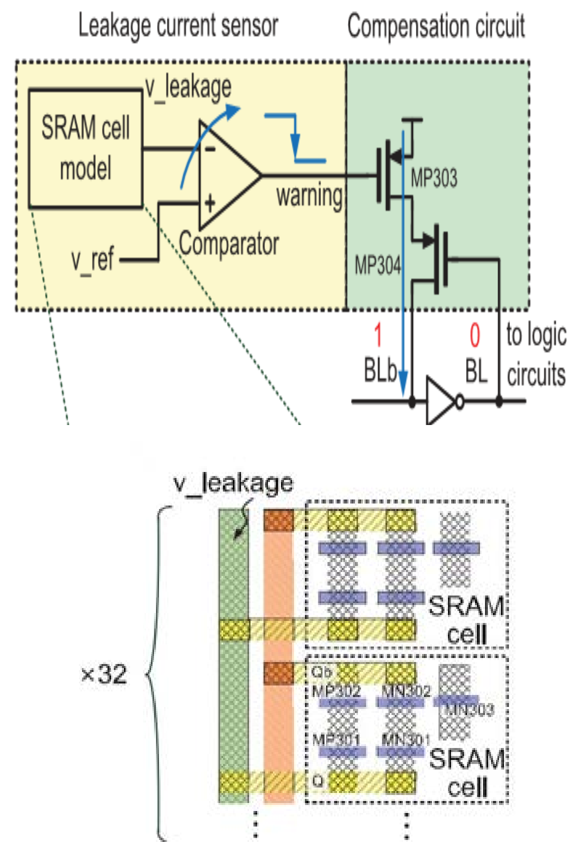

Fig.8 Schematics of leakage current sensor and compensation circuit.

Fig.8 Show the schematics of leakage current sensor and compensation circuit. A leakage current sensor consists of an SRAM cell model and a comparator. Since a larger leakage will result in low operating frequency, high power consumption, and even status flip in the SRAM cell. Comparator will notify a warning signal to activate the following compensation circuit. A Compensation circuit will speed up the read operation of SRAM if the leakage is detected and confirmed. SRAM cell model is used as a leakage monitor generating a voltage proportional to the leakage current, v_leakage, for comparator. If v_leakage is higher than v_ref, comparator will notify a warning signal to activate the following compensation circuit.

In this paper, we couple the node Q of 32 SRAM cells together and turn OFF all transistors to serve as the SRAM cell model. The reason is when the nodes Q of many SRAM cell are coupled together, the corresponding leakages of these cells are steered to the same node such that the common Q node voltage, v_leakage, will be pulled high almost proportionally.

B. Read Delay Compensation

The details of the leakage compensation are as follows.

Step 1: v_leakage rises to indicate that the SRAM cell model is suffered from leakage currents.

Step 2: Once if v_leakage is higher than v_ref, comparator pulls low the warning signal.

Step 3: As soon as the warning drops, MP303 in compensation circuit is turned ON to pull-up BLb such that BL drops fast. In other words, a positive feedback is used to speed up the read access.

since the BLb will be predischarged at the beginning of each read operation, this compensate operation only operates, while data bit 0 is accessed. When reading data bit 1, it stays the same. Besides, the charging speed of the proposed compensation circuit is determined by the size of MP303 and MP304.

C. Build-In Self-Test

It is a mechanism that permits a machine to self test. The main purpose of BIST to reduces the complexity, and thereby decrease the cost .And reduces the complexity of the test/probe setup, by reducing the number of I/O signals that must be driven under tester control. A well-known basic memory testing methodology is the BIST circuit. The BIST circuit in this design is implemented based on March C-algorithm. March C-algorithm is a popular testing algorithm, which has medium fault coverage and complexity. It can detect stuck-at fault, transition fault, address-decoder fault, and coupling fault.

3) IMPLEMENTATION AND MEASUREMENT

To ensure the functionality and performance of the proposed SRAM cell, the dynamic noise margin (DNM) and SNM of the proposed SRAM cell, respectively, by simulations. The DNM is ~0.3 V, which means that the state of the stored bit will not be interfered as long as the amplitude of the noise is lower than 0.3 V. the all-PT-corner simulation results of SRAM.

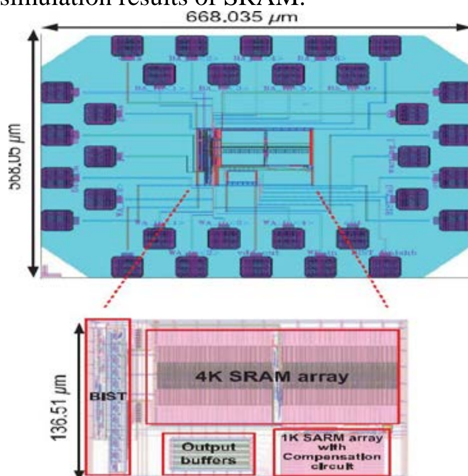

Fig.9 Layout of the proposed design SRAM

Layout of the proposed design SRAM in shown in fig.9. Two SRAM arrays are carried on the same die sharing common row decoder and column decoder. Notably, the 1-kb SRAM array with compensation only needs bit_addr, while the 4-kb SRAM array without compensation needs bit_addr.

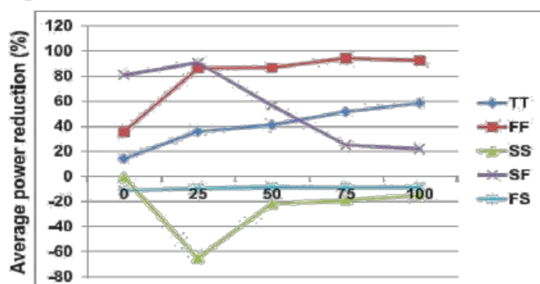

Fig.10 Improvement of power dissipation after compensation.

The leakage will slow down the entire read access, especially in the scenario of state 0 is to be read. Therefore, a compensation circuit consisting of two pMOS keepers, MP303 and MP304, speeds up the read operation such that the inverter and the following logic circuits can quickly pass the triode region to reduce power dissipation.

Fig.10 shows the average power dissipation reduction in different temperature and process corners. Notably, the power dissipation becomes bad at SS and FS corners, because the two pMOS keepers in a compensation circuit are in slow corner (S), which is turn slows down the read access. In summary, the mean average power dissipation is reduced by 27.86%. Notably, the overhead of the core area is only 3.64%.

The MATLAB turns to simulation and implement results Fig.11 describes when design with the MATLAB coding use to show the leakage current compensation.

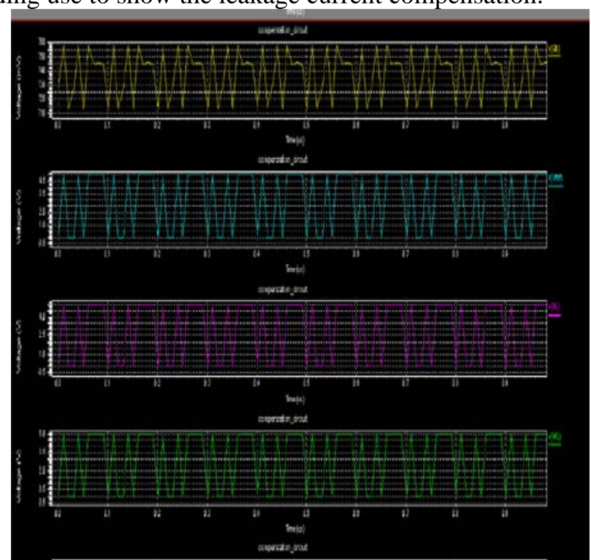
Fig.11 Waveform Analysis with MATLAB coding

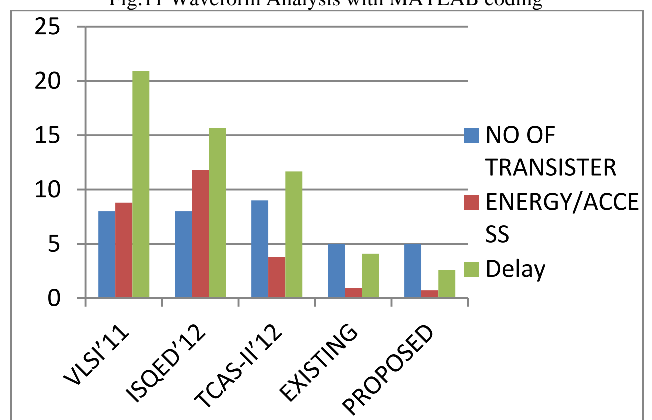

Fig.12 Comparisons of Existing & Proposed methods.

4) CONCLUSION

The read delay compensation design for 5T with transmission gate low supply voltage SRAM present in this paper. A novel five transistor SRAM cell presented for application in high speed, low power cache. It is used to enhance the write ability of the SRAM cell using transmission gates and further modification is done in the write assist circuit to reduces the power consumption and delay. The proposed circuit gives better result. The

compensation circuit consist of leakage current sensor and current compensation circuit. The SRAM cell optimized based on PDP.

The leakage current sensor, which generates a warning signal if the leakage is over a predefined threshold, and a compensation circuit following the sensor, which will be activated to speed up the read operation. The proposed Static Random-Access Memory is implemented using the TSMC 40-nm (CMOS) Complementary Metal Oxide Semiconductor logic technology. The energy per access is measured to be 0.9411 pJ given a 600-mV power supply and a 54-MHz system clock rate. The reduce power delay 2.58ns and 27.86% of the average power dissipation reduced.

ACKNOWLEDGMENT

The authors acknowledge the contributions of the students, faculty of M.P.Nachimuthu M.Jaganathan Engineering College for helping in the design of check circuitry, and for tool support. The authors also thank the anonymous reviewers for their thoughtful comments that helped to improve this paper. The authors would like to thank the anonymous reviewers for their constructive critique from which this paper greatly benefited.

REFERENCES

[1] Chua-Chin Wang,Deng-Shain Wang,China-Hsiang Liao,sih-Yu Chen,(2016),"A Leakage compensation Design for Low Supply Voltage SRAM," IEEE Senior Member.

[2] Agawa.K, Hara.H, Takayanagi.T, and Kuroda.T,(2001) "A bitline leakage compensation scheme for low-voltage SRAMs," IEEE Journel Solid-StateCircuits. vol. 36, no. 5, pp. 726–734, May 2001

[3] Chen.J, Clark. L.T, and Cao.Y, (2006)"Maximum Ultra-low voltage circuit design in the presence of variations," IEEE Circuits Devices Mag. vol. 21, no. 6, pp. 12–20, Jan./Feb. 2006.

[4] Chen.S and Wang.C-C., (2012)"Single-ended disturb-free 5T loadless SRAM cell using 90 nm CMOS process," inProc. IEEE Int. Conf.IC Design Technol. May/Jun. 2012, pp. 1–4

[5] Frustaci.F, Corsonello.P, Perri.S, and Cocorullo.G,(2006) "Techniquesfor leakage energy reduction in deep sub micrometer cache memories,"IEEE Trans. Very Large Scale Integr. Vol.14,no.1,p,1238-1249,nov.2006

[6] Goudarzi.M and Ishihara.T,(2010)"SRAM leakage reduction by row/columnredundancy under random within-die delay variation," IEEE Trans.Very Large Scale Integr. vol. 18, no. 12, pp. 1660–1671, dec.2010.

[7] Moradi.F, Wisland.D.T, Aunet.S, Mahmoodi.H, and Cao.T.V,(2008)"65 nm sub-threshold 11T-SRAM for ultra-low voltage applications,"in Proc. IEEE Int. Syst. ., Sep. 2008, pp. 113–118.

BIOGRAPHY

R.Mohan completed his M.E Applied Electronics in Karunya Institute of Technology, Anna University, Completed his B.E Electrical and Electronics Engineering, Bharathiyar University, Coimbatore. Now, He is working as a Associate Professor in ECE department in M.P.Nachimuthu M.Jaganathan Engineering College, Erode, India and have 11 years of teaching experience. He has published more than 12 research papers in various national and international conference proceedings. His area of interest includes VLSI Design, Embedded and Low power.

Vinitha.K.V pursuing M.E VLSI Design in M.P.Nachimuthu M.Jaganathan Engineering College Erode, Tamilnad,India and she completed her B.E degree in Electronics and Communication Engineering in Sri Ramanathan Engineering College 2015,Vijayamangalam Tamilnadu,India.Her areas of interest in research are VLSI architectures,Embedded Systems and Digital Electronics.