TESTING THE FUNCTIONAL AND MANUFACTURING DEFECTS OF CHIP USING JTAG (&) LABVIEW

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Abstract— *JTAG is a method for testing interconnects (wire lines) on printed circuit boards or sub-blocks inside an integrated circuit. The effect of testing will affect various parameter of device under test. The statistics which should be observed while testing the circuit such as test coverage, testing time, fault coverage, test vectors, testing power, delay. It is difficult to process the testing with all the criteria into the account. In order to make the process easier*

Keywords— JTAG Protocol; Boundary Scan; IEEE 1149.1 Standard; LabVIEW; RS232; Gates; TAP; PCB

1. INTRODUCTION

The high performance LA-ispMACH 4000V/Z automotive family from Lattice offers a Super-FAST CPLD solution that is tested and qualified to the AEC-Q100 standard. The family is a blend of Lattice's two most popular architectures: the ispLSI®2000 and ispMACH4A.

Retaining the best of both families, the LA-ispMACH4000V/Z architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The LA-ispMACH 4000V/Z automotive family combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The LA-ispMACH 4000V/Z automotive family offers densities ranging from 32 to 128 macro cells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) packages ranging from 44 to 144 pins. The LA-ispMACH 4000V/Z automotive family has enhanced system integration capabilities

It supports 3.3V (4000V and 1.8V (4000Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant.

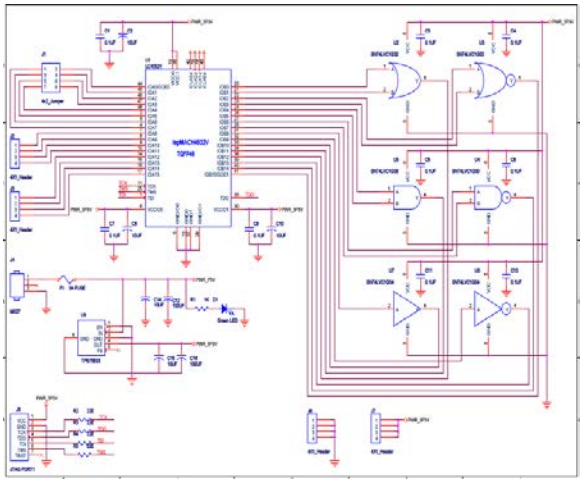
The LAispMACH 4000V/Z also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The LA-ispMACH 4000V/Z automotive family is in-system programmable through the IEEE Standard 1532 interface

Board Level Design for Testability (DFT):

The design rules discussed in this document are guidelines that support optimal test coverage and reliable execution of Boundary Scan tests. Circumstances of a specific printed circuit board (such as signal trace layout, functionality, cost considerations, available "real estate" on the PCB) may necessitate deviations from these guidelines.

A basic understanding of IEEE 1149.1, Standard Test Access Port and Boundary Scan Architecture, often referred to in short as JTAG or Boundary Scan, are beneficial. Of particular interest are the Test Access Port (TAP) signals, the workings of the TAP controller, and Boundary Scan capabilities of I/O pins

2. SCHEMATIC DIAGRAM



3. FUNCTIONAL BLOCK DIAGRAM

A.TAP Controller

The IEEE-1149.1 standard defines a common interface for JTAG control, called the Test Access Port (TAP). The TAP interface is a set of output and input pins that allows serially inserting and extracting internal register data, and at the same time to control the embedded JTAG controller's state. Since the data is processed serially, the registers that will be read or written through the TAP are arranged in a daisy-chain fashion. This structure is called a boundary scan chain. Chains are not bound to a single physical device.

The TAP interface was designed such that multiple ICs that support JTAG may be linked together to create compound chains. Originally, as the JTAG name implies, the interface was conceived to perform electrical connectivity tests

between components in a board; however in time developers found other uses for it.
The signals present in a TAP interface. The TDI, TDO, TMS and TCK signals are mandatory. The TRST signal is optional since it is always possible to soft reset the TAP machine clocking five ones into the TMS pin ('11111').

B. Test clock input (TCK)

The test clock input (TCK) provides the clock for the test logic defined by this standard

Specifications Rules

Stored-state devices contained in the test logic shall retain their state indefinitely when the signal applied to TCK is stopped at 0.

Recommendations

Since TCK inputs for many components may be controlled from a single driver, care should be taken to ensure that the load presented by TCK is as small as possible

C. Test mode select input (TMS)

The signal received at TMS is decoded by the TAP controller to control test operations.

Specifications Rules

- The signal presented at TMS shall be sampled by the test logic on the rising edge of TCK.
- The design of the circuitry fed from TMS shall be such that a un driven input produces a logical response identical to the application of a logic 1.

Recommendations

Since the TMS inputs for many components may be controlled from a single driver, care should be taken to ensure that the load presented by TMS is as small as possible.

D. Test data input (TDI)

Serial test instructions and data are received by the test logic at TDI.

Specifications Rules

- The signal presented at TDI shall be sampled into the test logic on the rising edge of TCK.
- The design of the circuitry fed from TDI shall be such that an undriven input produces a logical response identical to the application of a logic 1.
- When data is being shifted from TDI toward TDO, test data received at TDI shall appear without inversion at TDO after a number of rising and falling edges of TCK determined by the length of the instruction or test data register selected.

E. Test data output (TDO)

TDO is the serial output for test instructions and data from the test logic defined in this standard.

Specifications Rules

- Changes in the state of the signal driven through TDO shall occur only on the falling edge of TCK.
- The TDO driver shall be set to its inactive drive state except when the scanning of data is in progress

F. Test reset input (TRST)*

The optional TRST* input provides for asynchronous initialization of the TAP controller

Specifications Rules

- If TRST* is included in the TAP, the TAP controller shall be asynchronously reset to the Test-Logic-Reset controller state when a logic 0 is applied to TRST*.
- NOTE—As a result of this event, all other test logic in the component is asynchronously reset to the state required in the Test-Logic-Reset controller state.
- If TRST* is included in the TAP, the design of the circuitry fed from that input shall be such that an undriven input produces a logical response identical to the application of a logic 1.
- TRST* shall not be used to initialize any system logic within the component.

Recommendations

To ensure deterministic operation of the test logic, TMS should be held at 1 while the signal applied at TRST* changes from 0 to 1

G. TAP Controller

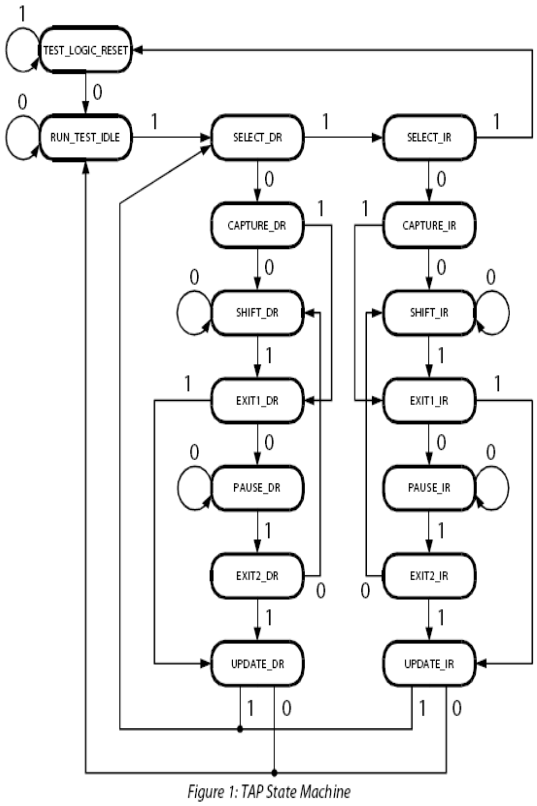


Figure 1: TAP State Machine

H. Easy System Integration

- Superior solution for power sensitive consumer applications
- Input pull-up, pull-down or bus-keeper
- Programmable output slew rate
- 3.3V PCI compatible
- IEEE 1149.1 boundary scan testable

I. SINGLE 2-INPUT POSITIVE NAND GATE
Description

- This single 2-input positive-NAND gate is designed for 1.65-V to 5.5-V VCC operation.
- The SN74LVC1G00 performs the Boolean function
- The CMOS device has high output drive while maintaining the low static power dissipation over a board VCC operating range.

J. SINGLE 2-INPUT POSITIVE AND-OR GATE
Description

- The SN74LVC1G0832 device is a single 2-input positive AND-OR gate
- It performs the Boolean function Y = (A • B) + C.
- This device is designed for 1.65-V to 5.5-V VCC operation

K. SINGLE 2-INPUT POSITIVE NOR GATE
Description

- This device is designed for 1.65-V to 5.5-V VCC operation.
- The SN74LVC1G02 performs the Boolean function Y = A + B or Y = A • B in positive logic.
- The SN74LVC1G02 device is a single 2-input positive NOR gate

L.SINGLE 2-INPUT POSITIVE BUFFER GATE
Description

- The SN74LVC1G34 device performs the Boolean function Y = A in positive logic.
- This single buffer gate is designed for 1.65-V to 5.5-V VCC operation.
- TheSN74LVC1G34 device is a single 2-input positive Buffer gate

M. SINGLE 2-INPUT POSITIVE Single Inverter GATE Description

- The SN74LVC1G04 device is a single 2-input positive Inverter gate
- The SN74LVC1G04 device performs the Boolean function Y = A in positive logic.
- This single inverter gate is designed for 1.65-V to 5.5-V VCC operation

N. Applications

- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Wireless Headset, Keyboard, and Mouse
- TV: LCD/Digital and High-Definition (HDTV)
- Video Analytics: Serve
- Tablet: Enterprise

O. Voltage regulator (TPS75533) Description

The TPS75533 of 5-A low dropout (LDO) regulators contains four fixed voltage option regulators with integrated power-good (PG) and an adjustable voltage option regulator. These devices are capable of supplying 5 A of output current with a dropout of 250 mV (TPS75533). Therefore, the device is capable of performing a 3.3-V to 2.5-V conversion. Quiescent current is 125 μA at full load and drops down to less than 1 μA when the device is disabled. The TPS75533 is designed to have fast transient response for large load current changes.

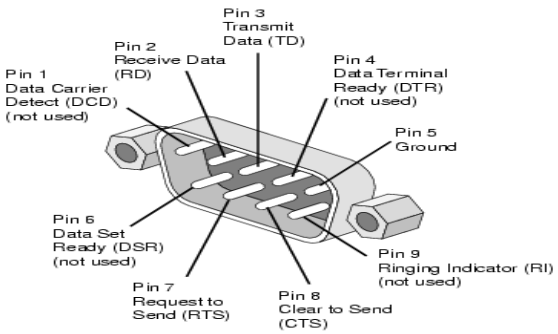
Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 250 mV at an output current of 5 A for the TPS75533) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 125 μA over the full range of output current).

P.RS-232

In telecommunications, RS-232 (Recommended Standard 232) is the traditional name for a series of standards for serial binary single-ended data and control signals connecting between a DTE (Data Terminal Equipment) and a DCE (Data Circuit-terminating Equipment). It is commonly used in computer serial ports. The standard defines the electrical characteristics and timing of signals, the meaning of signals, and the physical size and pin out of connectors.

An RS-232 port was once a standard feature of a personal computer for connections to modems, printers, mice, data storage, un-interruptible power supplies, and other peripheral devices. However, the limited transmission speed, relatively large voltage swing, and large standard connectors motivated development of the universal serial bus which has displaced RS-232 from most of its peripheral interface roles.

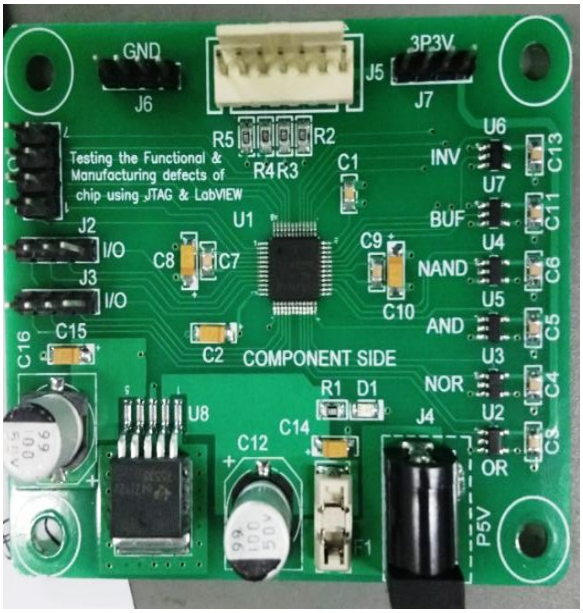
Q. Pin Configuration



R.RELAY

A relay is an electrically operated switch. Many relays use an electromagnet to operate a switching mechanism mechanically, but other operating principles are also used. Relays are used where it is necessary to control a circuit by a low-power signal (with complete electrical isolation between control and controlled circuits), or where several circuits must be controlled by one signal. The first relays were used in long distance telegraph circuits, repeating the signal coming in from one circuit and re-transmitting it to another. Relays were used extensively in telephone exchanges and early computers to perform logical operations

4. FUNCTIONALITY BOARD



5. SOFTWARE

5.1 LabVIEW

Laboratory Virtual Instrument Engineering Workbench (LabVIEW) is a system-design platform and development environment for a visual programming language from National Instruments

5.2 Each VI has three components

- Block diagram
- Front panel
- Connector panel

6. CONCLUSION

Testing the chips is a natural extension to the board level external testing that already is being performed. There is much benefit of reuse/salvage of existing tests to obtain deterministic test coverage metrics ensuring a quantitative level of quality assurance. The algorithm for test scheduling of SICs with two chips is extended to SICs with any number of chips forming the stack

The proposed test procedure can be further developed to include the testing of other data registers such as the Bypass register, and ID register, by executing the BYPASS, and the IDCODE instructions

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