HIGH SPEED CLOCK SYNTHESIS WITH LOW POWER CURRENT MODE DOUBLE EDGE TRIGGERED FLIPFLOP

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Abstract*—Most of the present day systems are fully based on clocks. In a high performance Very Large Scale Integrated Circuit (VLSI) design the Clock Distribution Network (CDN) consumes a significant amount of power. New circuit approaches Current Mode (CM) logic which saves significant amount power and has less complexity compared to Voltage Mode (VM) circuit. This CM scheme uses a low power Single Edge Triggered Flip-Flop (SETFF) combined with current pulse generator that is called CMSETFF provide one-to-many signalling which is very useful for CDN. Hence this CM CDN can reduce significant amount of power when compared to VM CDN. To improve the overall Speed of CDN from existing method of CMSETFF, the proposed method uses CMDETFF. Hence the delay of proposed CMDETFF is 50% very low when compared to CMSETFF so that the speed of CDN has been increased with low power.*

1. INTRODUCTION

In electronics and especially synchronous digital circuits, a clock signal is a particular type of signal that oscillates between a high and a low state and is used like a metronome to coordinate actions of digital circuits. A clock signal is produced by a clock generator. Although more complex arrangements are used, the most common clock signal is in the form of a square wave with a 50% duty cycle, usually with a fixed, constant frequency. Circuits using the clock signal for synchronization may become active at either the rising edge, falling edge, or, in the case of double data rate, both in the rising and in the falling edges of the clock cycle.

Power is a primary concern in all sorts of circuits. Clock Distribution Network (CDN) is an essential element of synchronous circuit and significant power consumer. CDN is defined as distribution of clock signal from the global clock generator to all elements which are connected in that network. In a synchronous digital system, the clock signal is used to define a time reference for the movement of data within that system. Since this function is vital to the operation of a synchronous system, much attention has been given to the characteristics of these clock signals and the networks used in their distribution. Clock signals are often regarded as simple control signals; however, these signals have some very special characteristics and attributes. Clock signals are typically loaded with the greatest fan-out, travel over the longest distances, and operate at the highest speeds of any signal, either control or data, within the entire system. Since the data signals are provided with a temporal reference by the clock signals, the clock waveforms must be particularly clean and sharp. Furthermore, these clock signals are particularly affected by technology scaling, in that long global interconnect lines become much more highly resistive as line dimensions are decreased. This increased line resistance is one of the primary reasons for the growing importance of clock distribution on synchronous performance. Finally, the control of any differences in the delay of the clock signals can severely limit the maximum performance of the entire system as well as create catastrophic race conditions in which an incorrect data signal may latch within a register.

2. EXISTING METHOD

In one-to-many current mode signalling scheme, a transmitter which is designed using NAND-NOR design and the Single Edge Triggered Current Mode Pulsed Flip-Flop (SETCMPFF) is used.

3. DISADVANTANGE OF EXISTING METHOD

The delay of existing CMSETFF CDN is 10.05 ns which is very high delay when compared with proposed CMDETFF. The power consumption of CMSETFF is 1.4928watts.

4. PROPOSED METHOD

If the sampling of the input is performed in both rising and falling edge of clock (Double Edge Triggered), then for same application and operational speed, the frequency of the clock can be half of the clock frequency of SETFF. So that the proposed method uses a CMDETFF instead of CMSETFF for increasing the overall speed of CDN with low power and delay.

A. BLOCK DIAGRAM

The block diagram of proposed clock distribution network is shown in Fig 1. This CDN is used in H-tree model and to transmit the clock signal at the receiver.

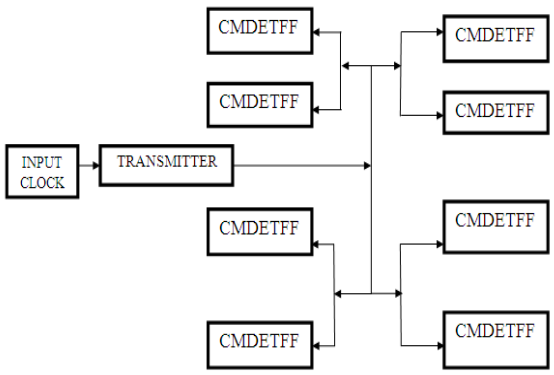


Fig.1 Block Diagram of proposed CDN

B. BLOCK DIAGRAM OF PROPOSED CMDETFF

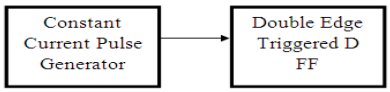


Fig.2 Block diagram of proposed CMDETFF

A low power CMDETFF is combined with current pulse Generator to do the function of CDN. Here Fig.1 describes the overall function of CDN and Fig.2 represents the proposed CMDETFF.

C. TRANSMITTER

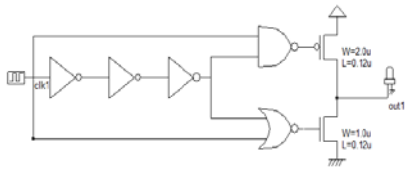


Fig.3 NAND-NOR Transmitter

NAND-NOR transmitter is used to produce the current to the transmission line to distribute the current to all the CMDETFF. In order to integrate the CMPFF with Enable, a transmitter provides a push pull current into the clock network and distributes required amount of current to each CMPFFE. Our proposed CM CDN with transmitter, interconnect, and CMPFFE is shown in Fig. 1. The transmitter receives a traditional voltage clock from a global clock generator at the root of H-tree network and supplies a pulsed current to an interconnect which is held at a near constant voltage. The CDN is a symmetric H-tree with equal impedances in each branch so that current is distributed equally to each CMPFFE leaf node.

The NAND gate uses the clock signal and a delayed inverted clock signal, as inputs to generate a small negative pulse to briefly turn on M. Hence, the PMOS transistor briefly sources charge from the supply while the NMOS is off. Similarly, the NOR gate utilizes the negative edge of the clock to briefly turn on M2. Hence, the NMOS transistor briefly sinks current while the M1 is off. The non overlapping input signal from the NAND-NOR gates remove any short circuit current from the transmitter.

The transmitter M1 and M2 device sizes are adjusted to supply/sink charge into/from the CDN. Depending on the size of load (number of sinks) and size of chip, the device sizes need to adjusted. The root wire of CDN carry current that is distributed to all branches so the sizing CDN wires are critical for both performance and reliability. If the resistance of the wire is to high, the current waveform magnitude and period will be distorted and affect performance of the CMPFFEs. The wire width must also consider electromigration effects while carrying a total current to drive all the flip-flops with the required current amplitude and duration.

D. CURRENT PULSE GENERATOR

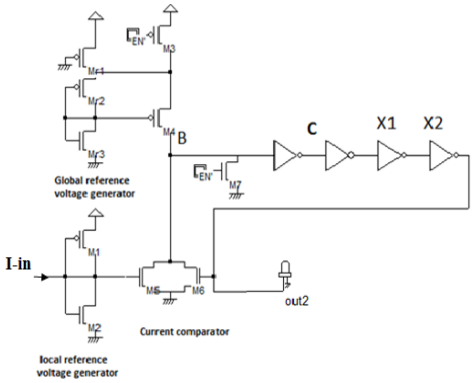


Fig.4 Current Pulse Generator

The Current Pulse Generator uses a global reference voltage generator, current comparator and inverters. The current comparator compares the current from the global reference voltage generator and current from the transmitter to produce the current pulses. This current pulse amplified using inverters. This amplified current pulse is used to trigger the DETFF.

E. DOUBLE EDGE TRIGGERED FF

DETFF uses the current pulse and operated on both the edges of clock signal. By using DETFF the clock frequency can be halved to achieve the same computational throughput compared to SETFF. This results in overall system power reduction because clock distribution is a major source of power consumption in a synchronous computation system. The proposed DETFF consists of exclusive-OR(XOR) gate and a single negative level triggered latch. This clock has the double the frequency of the system-wide clock signal, thereby ensuring that a new data value is stored into the latch at each edge of the system-wide clock signal. The original clock signal coming from the current pulse generator labelled as X is inverted and delayed by a certain amount of time to produce signal labelled Y. Performing XOR operation on the signals X and Y yields the desired clock signal whose frequency is double the frequency of original signal which is coming from the Current Pulse Generator. Observe that the duty cycle of the clock signal coming from the XOR gate is much less than 50% since this signal is low for a short period of time. Therefore, the negative level-sensitive latch is transparent for a very short amount of time, making it appear as if it was an edge-sensitive flip-flop.

5. SOFTWARE USED

- Tanner EDA (Electronic Design Automation) - V13.0
- Xilinx ISE (Integrated Synthesis Environment) - 9.1

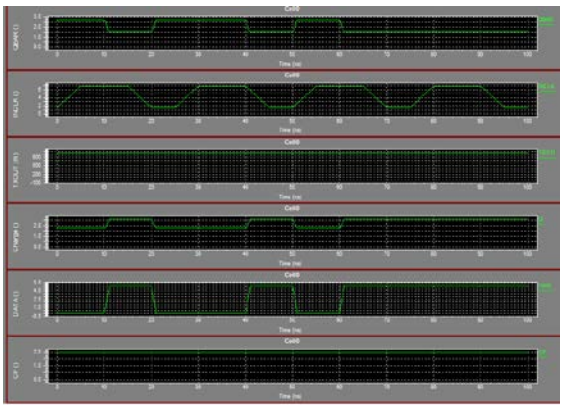
6. HARDWARE USED

FPGA(Field Programmable Gate Array) Spartan-3E

7. ADVANTAGES

Delay of proposed CMDETFF is 5.5 ns which is very low delay when compared to CMSETFF. So the speed of CDN has been improved. Power consumption of CMDETFF is 1.34watts which is also low when compared to existing method.

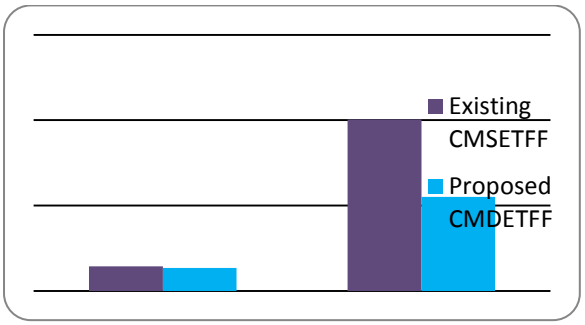
8. OUTPUT



9. PARAMETER ANALYSIS

S.NO	PARAMETER	EXISTING CMSETFF CDN	PROPOSED CMDETFF CDN
1	DELAY	10.05 ns	5.5 ns
2	POWER	1.4328 watts	1.348 watts

10. COMPARSION OUTPUT



11. CONCLUSION

The proposed CMDETFF is 55% faster and consumes 7 % less power when compared to a CMSETFF. The symmetric H tree provides zero clock skew which is suitable for high speed applications. The clock distribution using flip-flop is used for one to many clock distribution. This also neglects the use of complex current mode receiver.

12. FUTURE SCOPE

The future work of proposed method is in addition to high speed and low power. The CDN can also need to provide much area reduction through which more receiver i.e a FFs can be placed on a single chip.

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BIOGRAPHY

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