A HIGH PERFORMANCE DADDA MULTIPLIER USING 5:2 COMPRESSORS

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Abstract*—In this paper 5:2 Compressor are designed to analyze the Dadda Multiplier based on area, low power consumption and delay. Multiplication is a fundamental operation is most of the signal processing algorithms. Multipliers have large area and high speed operation. To reduction the number stages in dadda multiplier by using 5:2 compressors. The power consumption of the 5:2 compressor is very low by using the exact design of the compressor. The speed of the circuits is high because the delay of the circuit is low compared to 4:2 compressor. To analyze a high speed and low power consumption using the Tanner EDA tool and hardware implementation to be done in FPGA using Xilinx ISE 9.1i.*

1. INTRODUCTION

The Dadda Multiplier is a hardware multiplier. It is similar to Wallace Multiplier, but it is slightly faster and requires less gates. Dadda Multiplier reduces the number of rows as much as possible on each layer. Dadda Multiplier is less expensive when compared to Wallace Multiplier. Dadda multiplier do as few reduction as possible. The five dual-quality reconfigurable approximate 5:2 compressors,which provide the ability of switching between exact and approximate operating modes during the run time. 5:2 compressor is basic element for high speed and high accuracy multiplier. In the existing method, when compared to 5:2 compressors the speed of the 4:2 compressor in low because the delay of the circuit is high and the power consumption of 4:2 compressor is high. In order to overcome the drawbacks the 5:2 compressor design is proposed. 5:2 compressor are capable of working with the low power consumption and the speed of the compressor is high compared to the existing method.

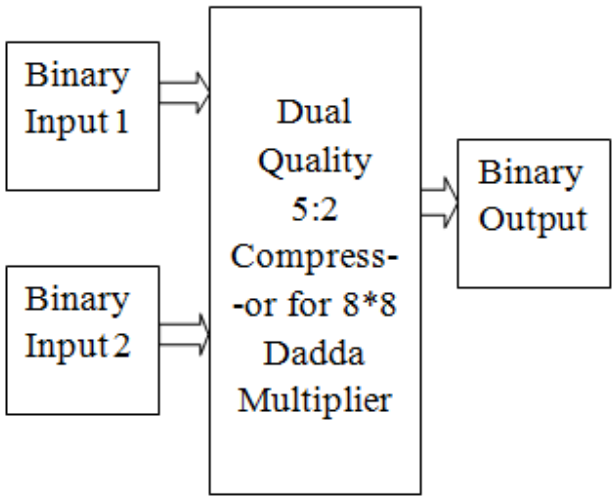

Fig.1 Block Diagram of Dadda Multiplier

As the weightage of sum bits 1 and the weightage of carry bits is 2 of conventional compressors, so the result that produced by these compressors are connect but not in proper binary form. when these conventional compressors are used in multiplier to achieve high speed then one half adder , full adder is required per compressor to process those carry bits. Thus it lampers the speed of operation.so the conventional compressors requires one more half adder, full adder to get the final result and this eventually adds more delay and power to the reported results.

The Dadda Multiplier is a hardware multiplier as shown in fig 1. It is similar to Wallace Multiplier,but it is slightly faster.In Dadda Multiplier that reduce the number of rows as much as possible on each layer.

2. EXISTING METHOD

A four dual-quality reconfigurable approximate 4:2 compressors, provide the ability of switching between the exact and approximate operating modes during the runtime. Each of these compressors has its own level of accuracy. Different delays and power dissipations in the approximation and exact modes.

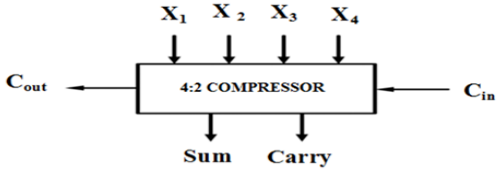

Fig.2 Block Diagram of 4:2 Compressor

The 4:2 compressor structure, actually compresses five partial products bits into three as shown in fig 2. The four inputs X_1, X_2, X_3, X_4 and the output Sum have the same weight.

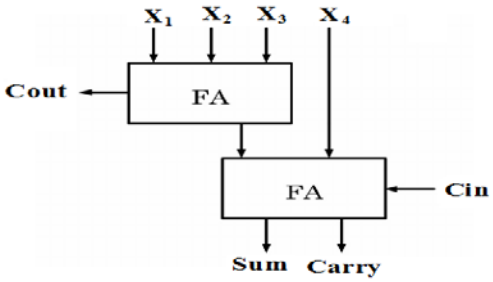

Fig.3 Conventional Diagram of 4:2 Compressor

- Exact compressor design using Full Adder

The 4:2 Compressor has 5 inputs X_1, X_2, X_3, X_4 and Cin to generate 3 outputs Sum, Carry and Cout as shown in fig 3. The input Cin is the output from a previous lower significant compressor and the Cout output is for the compressor in the next significant stage. The conventional approach to implement 4:2 compressors is with 2 connected in serially as shown in fig. 3.

3. PROPOSED METHOD

5:2 Compressors are used to reduce the area. Efficiencies of these compressors in a 32-bit Dadda multiplier are evaluated in a 250-nm standard CMOS technology by comparing their parameters with those of the state of the art approximated mode. The 5:2 Compressor are designed to analyze the Dadda Multiplier based on area, power consumption and delay. The compressor are widely used to speed up the process and reduce the partial product stages during the multiplication. To reduce power consumption using 250nm technology.

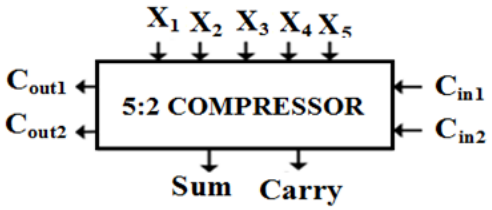

Fig. 4 Block Diagram of 5:2 Compressor

The compressor is a basic element for high speed and high accuracy multiplier. The block diagram of a 5:2 compressor shown in fig. 4 has seven inputs and four outputs. Five of the inputs are the primary inputs X_1, X_2, X_3, X_4 and X_5 and two other inputs, Cin l and Cin 2.

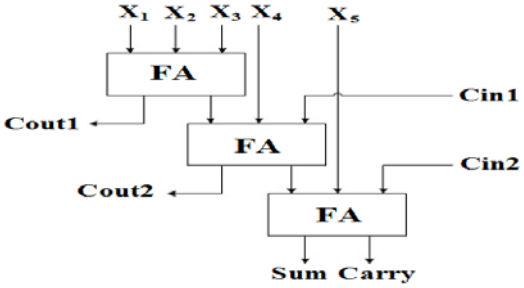

Fig. 5 Conventional Diagram of 5:2 Compressor

The exact 5:2 compressor is implemented by series connection of three full adder(FA) Blocks. The 5:2 compressor block has five inputs: X1, X2, X3, X4, X5, two carry input bits: Cin1 and Cin2 and produces 4 outputs: Sum, Carry, Cout1 and Cout2 as shown in fig. 5.

4. REDUCTION OF DADDA MULTIPLIER

COMPRESSOR

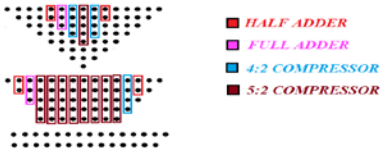

Fig. 6 Reduction Circuitry of an 8-bit Dadda Multiplier.

The general structure of reduction circuitryin an 8 bit Dadda Multiplier,which make of 5:2 Compressor as shown in fig 6. In step 1 C1, C2 needs no changes in them, but C3 has 3 bits. So, a half adder is required to reduce to 2 bits.In Step 2 C4 has 4 bits and carry from C3. Thus, a 4-2 compressor is needed.In Step 3 C5 to C12 has 5 bits including a carry from just preceding columns. So, a 5:2 compressor is required.In Step 4 C13 has 3 bits so using full adder is required to reduce it 2 bits.In Step5 C14 has 2 bits so using half adder is required to reduce it 2 bits.

5. COMPONENTS REQUIREMENTS

A)SOFTWARE USED

- Xilinx ISE (Integrated Synthesis Environment) 9.1i
- DSCH 2 (Digital Schematic)
- Tanner EDA (Electronic Design Automation) 13.0

B)HARDWARE USED

- FPGA (Field Programmable Gate Array) SPARTAN 3E

6. APPLICATIONS

- Digital Image Processing.
- Multimedia Application

7. SIMULATION RESULT OF PROPOSED METHOD

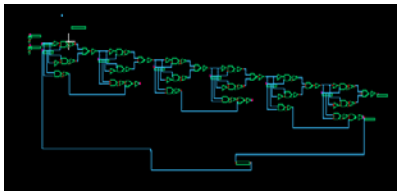

Fig. 7 Schematic Diagram of 5:2 Compressor

```
* BEGIN NON-GRAPHICAL DATA

Power Results
in gnd from time 0 to 1e-007
Average power consumed -> 2.899349e-005 watts
Max power 3.866308e-003 at time 9.1e-008
Min power 0.000000e+000 at time 0


* END NON-GRAPHICAL DATA


* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

delay = 2.5500e-008

* END NON-GRAPHICAL DATA
*
```

Fig. 8 Output File of 5:2 Compressor

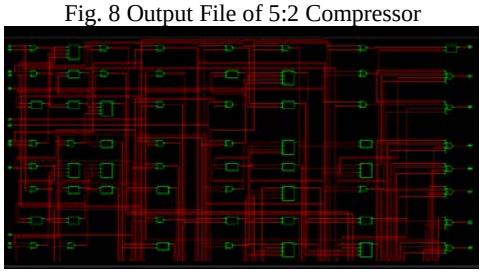

Fig. 9 RTL Schematic Diagram of Proposed Method

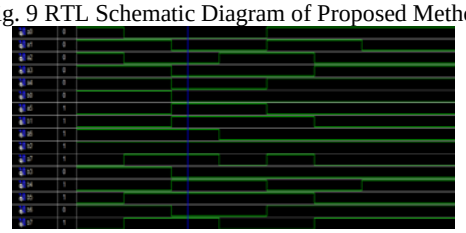

Fig. 10 Input Waveform

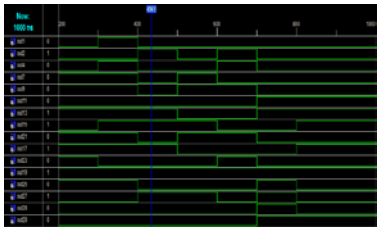

Fig. 11 Output Waveforms

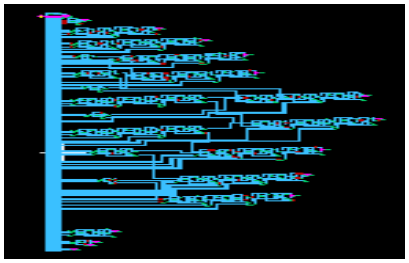

Fig. 12 Schematic Diagram of Dadda Muliplier using 5:2 Compressor

```
* BEGIN NON-GRAPHICAL DATA

Power Results
in gnd from time 0 to 1e-007
Average power consumed -> 2.139858e-004 watts
Max power 2.622390e-002 at time 6.1e-008
Min power 0.000000e+000 at time 0


* END NON-GRAPHICAL DATA


* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

delay = 1.5500e-008

* END NON-GRAPHICAL DATA
*
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Fig.13 Output File of Dadda Multiplier using 5:2 Compressor

8. EXPRIMENTAL RESULT

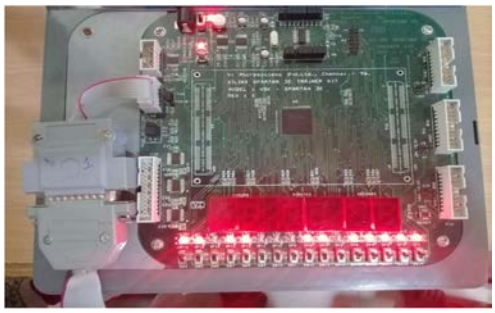

Fig. 14 Hardware Output of Dadda Multiplier

9. CONCLUSION

In this paper 5:2 compressor are designed to analyze the dada multiplier based on low power consumption and dealy.multiplication is a fundamental operation is most of the signal processing algorithms. Multipliers have large area and high speed operation. To reduction the number of stages in dada multiplier by using 5:2 compressors. The power consumption of the 5:2 compressors is very low by using the exact design of the compressor. The speed of the circuits is high because the delay of the circuit is low powered of 4:2 compressor.

In this paper designed,simulated, synthesized and implemented an 8-bit by 8-bit dada multiplier with improved algorithm only for the unsigned integers. However,the same concept can be used to realize multiplication of signed integers,signed real numbers and FPGU(Floating Point Arithmetic Unit). Further,the proposed algorithm can be applied for higher sizes of multiplier (16 by 16,32 by 32 and more).

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BIOGRAPHY

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