DESIGN OF SEQUENTIAL CIRCUITS USING ADIABATIC LOGIC

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Abstract— *In the modern world one of the biggest challenges is to reduce the power consumption in electronic devices which will lead to longer battery life while maintaining high performance. Reduction of power consumption can be done by low power design. This can be achieved by adiabatic logic technique. In this paper, conventional CMOS circuits and ECRL circuits for flip flop for SR, JK, D& T are designed using Cadence Virtuoso Tool at 45nm process technology &Stimulated using Spectre. Power consumption of CMOS & ECRL flip flop is compared and computed.*

Keywords— Adiabatic; CMOS; Power Analysis; ECRL; Flip Flop; 45nm Technology

1. INTRODUCTION

The Power dissipated in a CMOS circuit is the sum of dynamic power; short-circuit power and static or leakage power. The low power design states that the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power digital and analog circuit. In order to achieve this, low power design adiabatic logic is on such technique where using AC voltage supplies or power clock to recycle the energy of circuit instead of being dissipated as heat.

Classification of AL:

1) Partially/Quasi Adiabatic Logic
   1. ECRL (Efficient Charge Recovery Logic)
   2. CAL (Clocked CMOS Adiabatic Logic)
   3. TSEL (True Single Phase Adiabatic Logic)
   4. SCAL (Source-coupled Adiabatic Logic)
2) Fully Adiabatic Logic
   1. PAL (Pass-transistor Adiabatic Logic)
   2. Split-level Charge Recovery Logic (SCRL)

Efficient Charge Recovery Logic (ECRL) uses cross coupled PMOS transistors. It consists of two cross coupled transistors PM1 and PM2 and two N-functional blocks for the ECRL adiabatic logic block. Power clock (four phase clock supply) or AC voltage is used for ECRL gates, so as to recover and reuse the supplied energy. Both output and output bar generated.

CMOS (Complementary metal–oxide–semiconductor) is a technology for constructing integrated circuits. The words 'complementary-symmetry' refer to the fact that the typical design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors for logic functions.

In this paper we have designed the SR, JK & D flip-flop using CMOS and ECRL style of design and stimulated using spectre. The stimulated output waveform for CMOS and ECRL circuits is compared and noted the corresponding power consumption for CMOS and ECRL design.

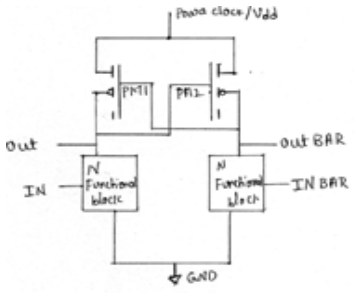

Fig 1: Basic Circuit of ECRL

2. CMOS SR CIRCUIT DESIGN

The CMOS SR circuit is implemented with four NAND gate instances as shown in figure 1. the CMOS circuit is responsive to S or R only if clk is high.

- If both input signals and the CLK signals are active high: i.e. the latch output Q will be set when CLK = 1, S= 1 and R = 0.
- Similarly, resetting of the latch will be done when CLK = 1, S = 0 and when CLK is low, the latch retains its present state.

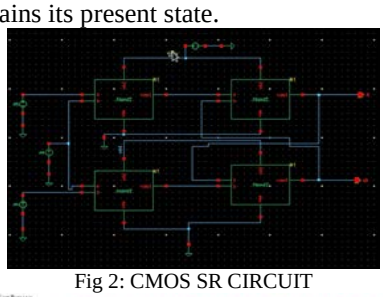

Fig 2: CMOS SR CIRCUIT

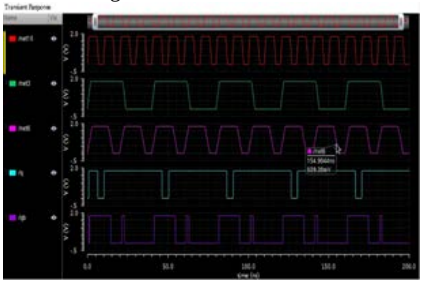

Fig 2: CMOS SR WAVEFORM

3. CMOS JK CIRCUIT DESIGN

The Circuit below shows a clocked JK, based on NAND gates. The disadvantage of an SR latch is that when both S and Rare high, its output state becomes in determinant. The JK latch eliminates this problem by using feedback from output to input, such that all input states are allowable.

- If J= 1 and K= 0, the latch will set on the next going clock edge, i.e. Q = 1, ¬¬Qb = 0.
- If J = 0 and K = 1, the latch will reset on the next going clock edge, i.e. Q = 1 and Qb= 0.
- If J = K = 1, the latch will toggle on the next going clock edge.
- If J = K = 0, the latch will hold its present state.

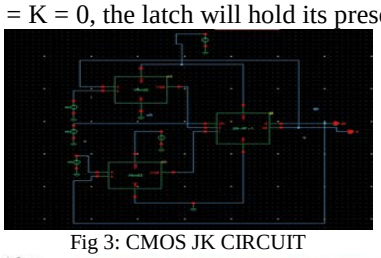

Fig 3: CMOS JK CIRCUIT

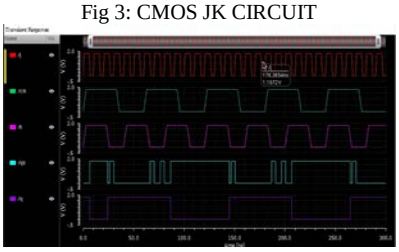

Fig 4: CMOS JK WAVEFORM

4. CMOS T CIRCUIT DESIGN

The CMOS implementation of T Input and output Circuit is shown below where both J and K input are tied to common input that is T input. The input can either take logic 1 or logic 0. If T takes the value of logic 1, the output Q will then change state or toggle. If T=0, the state will not change.

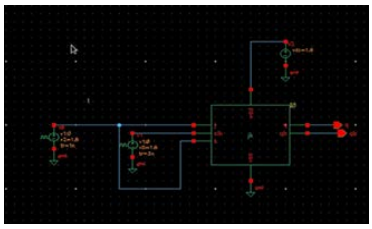

FIG 5: CMOS T CIRCUIT

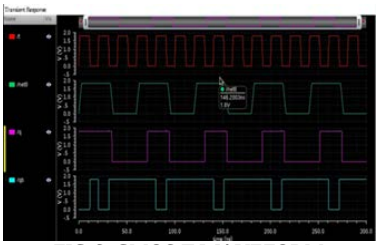

FIG 6: CMOS T WAVEFORM

5. CMOS D CKT DESIGN

The CMOS D Input and Output are simply a SR Input and output with the S and R connected by an inverter to the same inputs D shown in Circuit. The gate level representations of the D Input and Output are simply obtained by modifying the clocked NAND based SR Input and output circuit. The output Q assumes the value of the input D when the clock is active (i.e. for CLK= 1). When the clock signal goes to zero, the output will simply preserve its previous state.

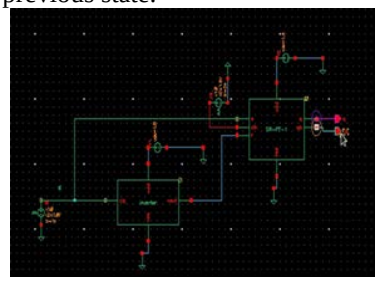

FIG 7: CMOS D CIRCUIT

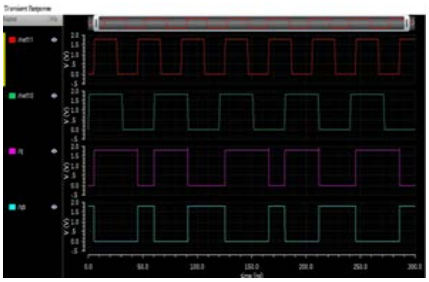

FIG 8: CMOS D WAVEFORM

6. ECRL SR CIRCUIT DESIGN

The SR ECRL input and output besides the PMOS loads (PM0, PM1) and the NMOS pull down transistors (NM2-NM5), there are two other NMOS transistors (NM0, NM1) along the feedback paths of the outputs Q and QB, respectively. The gates of NM0 and NM1 are connected to negative triggering. During the pre-charge/evaluate phase, if the output node Q swings 0 to CLK (representing a logic 1), the gate capacitance of NM3 will be charged to turn NM3 on. At the same time, NM4 will be turned 0 since its gate is connected to QB (which is at logic 0) via NM1. On the next clock cycle, if S= 1 and R= 0, or S= R= 0 (SET), QB will still be at 0 V by NM2 or NM3, while Q is at logic 1. If S = 0 and R = 1 (RESET), Q will be held at 0 V and the gate capacitance of NM3 will be discharged to 0V. With NM2 and NM3 turned 0, QB will be charged up to CLK by PM1.

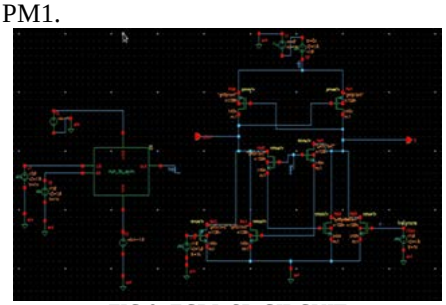

FIG 9: ECRL SR CIRCUIT

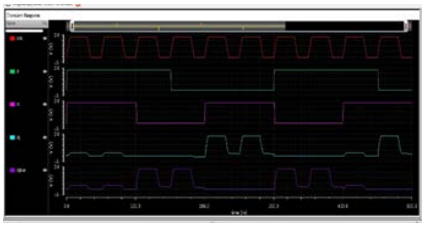

FIG 10: ECRL SR WAVEFORM

7. ECRL JK CIRCUIT DESIGN

The ECRL JK flip-flop is designed as Shown below. The simulated wave-forms are as shown below the CKT. It

consists of a basic JK flip-flop cell. The NMOS evaluation phase (NM1-NM12) in the basic cell represents the true and complementary logic of the JK flip-flop. During the Pre-charge phase, if the output node Q swings from 0 to CLK (representing a logic 1), QB pulls to logic 0 through (NM2-NM6-NM10). During the next clock cycle, when J = 1and K = 0 the outputs Q and QB is at logic1and logic 0 respectively. When J= 0 and K= 1, the outputs Q and QB will be logic0 and logic1, respectively.

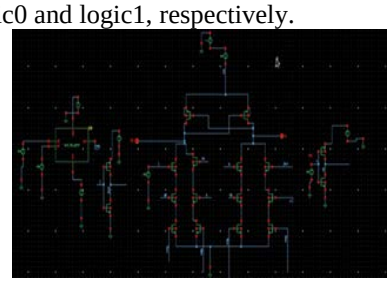

FIG 11: ECRL JK CIRCUIT

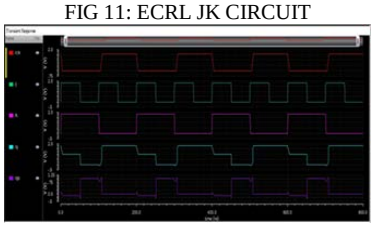

FIG 12: ECRL JK WAVEFORM

8. ECRL D CIRCUIT DESIGN

The D ECRL flip-flop circuit design is shown below and the simulated transient wave-forms are as shown below. Besides the PMOS loads (PM0, PM1) there are four NMOS pull down transistors (NM0-NM3). During the evaluate phase, when D= 1 and the negative triggering is high, node QB becomes low. This will turn PM1 'on' and we have Clk (high) in the Q output. The output is held during the hold phase. The energy delivered during the evaluate phase is recovered during the recovery phase by the discharging current through PM0. When D = 0 and the negative triggering is high, node Q takes low value and this will turn PM0 on and we have Clk in the QB output and the energy is recovered during the recovery phase.

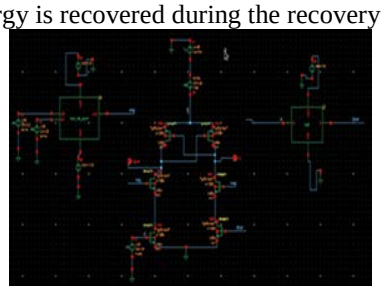

FIG 13: ECRL D CIRCUIT

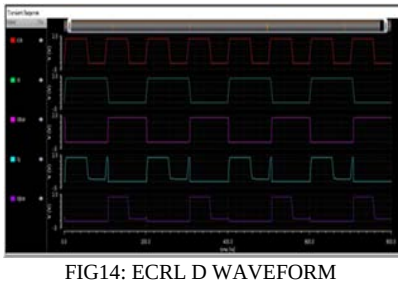

FIG14: ECRL D WAVEFORM

9. ECRL T CIRCUIT DESIGN

During evaluation phase T=1, negative trigger is applied Q becomes 0 and Q bar high (1) this makes PMOS1 on and when negative clock is applied the output is held during the hold phase. During the recovery phase the current through the PMOS0 uses the evaluation phase energy. When T=0 the negative trigger is applied the output will remain same.

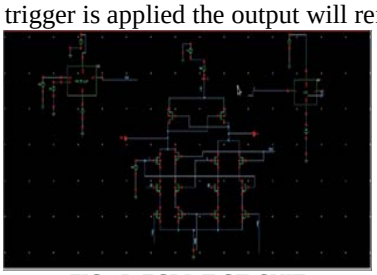

FIG 15: ECRL T CIRCUIT

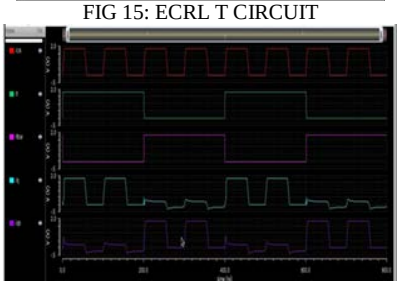

FIG 16: ECRL T WAVEFORM

10. POWER ANALYSIS [45NM TECHNOLOGY]

FLIP FLOP	POWER IN CMOS (uW)	POWER IN ECRL (uW)	% OF POWER REDUCATION
SR	22.60	0.022	22.57
JK	56.43	0.0005841	56.42
D	53.83	0.006042	53.81
T	57.65	0.005004	57.64

11. CONCLUSION

The above analysis, shows that power consumption of the ECRL adiabatic and CMOS sequential circuit. Negative edge triggering gives additional merits of reduce in clock skew and jitters, when compared with the positive edge trigger and pulsed flip flop. This analysis shows negative edge triggered ECRL circuit of SR, JK, D and T flip flop shows significant improvement in power consumption as that of CMOS based flip flop. This justifies that ECRL circuit design gives better performance with respect to CMOS circuit design as CMOS circuits dissipates more power than ECRL circuit.

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