A MULTILEVEL INVERTER TOPOLOGY FOR A FOUR-POLE INDUCTION-MOTOR DRIVE USING DC-LINK

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Abstract— *A multilevel inverter topology for a four-pole induction-motor drive is presented in this paper, which is constructed using the induction-motor stator winding arrangement. A single dc source with a less magnitude when compared with conventional five-level inverter topologies is used in this topology. Therefore, power balancing issues (which are major challenges in conventional multilevel inverters) are minimized. As this configuration uses a single dc source, it provides a path for zero-sequence currents because of the zero-sequence voltages present in the output, which will flow through the motor phase winding and power electronic switches. To minimize these zero-sequence currents, sine–triangle pulse width modulation (SPWM) is used, which will shift the lower order harmonics near to switching frequency in the linear modulation region. However, in the case of over modulation, harmonic voltages will be introduced close to the fundamental frequency. In this regard, a modified SPWM technique is proposed in this paper to operate the drive in the over modulation region up to the modulation index of 2 /√3. The proposed quad two-level inverter topology is experimentally verified with a laboratory prototype on a four-pole 5-hp induction motor. Experimental results show the effectiveness of the proposed topology in the complete linear modulation region and the over modulation region.*

Keywords— ***Back-to-Back Converter; Dynamic Performance; Induction Machine Drives; Open-End Winding and Unity Power Factor***

1. INTRODUCTION

The conventional topologies of multilevel inverter fundamentally are diode-clasped and capacitor-cinched sort . The former utilizes diodes to clasp the voltage level, and the recent uses extra capacitors to clip the voltage. The higher number of voltage levels can then be acquired; on the other hand, the circuit be-comes to a great degree intricate in these two topologies. An alternate sort of multilevel inverter is fell H-Bridge built by the arrangement association of H-Bridges . The fundamental circuit is like the established H-span DC–DC converter. The fell structure expands the framework dependability due to the same circuit cell, control structure and balance. How-ever, the disservices went up against by fell structure are more switches and various inputs. With a specific end goal to expand two voltage levels in staircase yield, a H-Bridge built by four force switches and an individual info are required. The oretically, fell H-Bridge can get staircase yield with any number of voltage levels, yet it is improper to the applications of expense sparing and information confinement.

Various studies have been performed to expand the quantity of voltage levels. An super capacitor (SC) based multilevel circuit can adequately expand the quantity of voltage levels. Notwithstanding, the control methodology is perplexing, and EMI issue gets to be more regrettable because of the intermittent data current. A solitary stage five-level pulsewidth-tweaked (PWM) inverter is constituted by a full scaffold of diodes, two capacitors and a switch. Be that as it may, it just furnishes yield with five voltage levels, and higher number of voltage levels is restricted by circuit struc-ture [16]. A SC-based fell inverter was given SC frontend and full extension backend. Notwithstanding, both entangled control and expanded parts utmost its application [17]. The further study was introduced utilizing arrangement/parallel transformation of SC. Then again, it is improper to the applications with HF out-put due to multicarrier PWM (MPWM). On the off chance that yield recurrence is around 20 kHz, the bearer recurrence achieves a few megahertz. To be specific, the transporter recurrence in MPWM is handfuls times of the yield recurrence. Since the bearer frequency decides the exchanging recurrence, a high exchanging misfortune is certain for the purpose of high-recurrence yield.

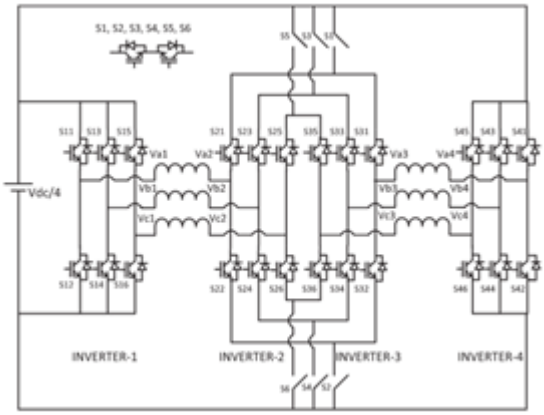


Fig 1: Block diagram of A Multilevel inverter topology for a four-pole induction-motor drive using DC-Link

A help multilevel inverter situated in fractional charging of SC can expand the quantity of voltage levels hypothetically. In any case, the control system is muddled to actualize incomplete charging [20]. Along these lines, it is a testing errand to present a SC-based multi-level

inverter with high-recurrence yield, low-yield harmonics, and high transformation productivity.

Taking into account the study circumstance previously stated, a novel multi-level inverter and straightforward tweak methodology are displayed to serve as HF force source. Whatever is left of this paper is sorted out as takes after.

2. CONTROL OF IM

Consider a symmetrical three-phase induction machine with stationary as-bs-cs axes at 2Π/3 angle apart, as shone in figure 3.2. Our gole is to transform the three-phase stationary reference frame (as-bs-cs) variables into two – phase stationary reference frame (ds-qs) variables and then these to synchronously rotating reference frame (de-qe), and vice versa.

Assume that the ds-qs axes are oriented at θ angle, as shown in figure 3.2. The voltages vdss and vqss can be resolved into as-bs-cs components and ca n be represented in matrix form as Dynamic D – Q model

Fig.2 Stationary frame a-b-c to ds-qs axes transformation

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta-120^{o}) & \sin(\theta-120^{o}) & 1 \\ \cos(\theta+120^{o}) & \sin(\theta+120^{o}) & 1 \end{bmatrix} \begin{bmatrix} v_{qs}^{s} \\ v_{ds}^{s} \\ v_{os}^{s} \end{bmatrix} \quad (3.1)$$

The corresponding inverse relation is

$$\begin{bmatrix} v_{qs}^{s} \\ v_{ds}^{s} \\ v_{os}^{s} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta-120^{o}) & \cos(\theta+120^{o}) \\ \sin\theta & \sin(\theta-120^{o}) & \sin(\theta+120^{o}) \\ 0.5 & 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} \quad (3.2)$$

Where Voss is added as the zero sequence component, which may or may not be present. We have considered voltage as the variable. The current and flux linkages can be transformed by similar equations. It is convenient to set θ = 0, so that the qs-axis is aligned with the as-axis. Ignoring the zero sequence components, the transformation relations can be simplified as

$$V_{as} = V_{qs}^{s} \quad (3.3)$$

$$V_{bs} = -(1/2)V_{qs}^{s} - (\sqrt{3}/2)\, V_{ds}^{s} \quad (3.4)$$

$$V_{cs} = -(1/2)\, V_{qs}^{s} + (\sqrt{3}/2)\, V_{ds}^{s} \quad (3.5)$$

$$V_{qs}^{s} = (2/3)\, V_{as} - (1/3)\, V_{bs} - (1/3)\, V_{cs} = \quad (3.6)$$

And inversely

$$V_{qs}^{s} = (2/3)\, V_{as} - (1/3)\, V_{bs} - (1/3)\, V_{cs} = V_{as} \quad (3.7)$$

$$V_{ds}^{s} = -(1/\sqrt{3})\, V_{bs} + (1/\sqrt{3})\, V_{cs} \quad (3.8)$$

3. PROPOSED SYSTEM

Power converters of different topologies have found wide applications in many grid interfaced systems including distributed power generation by renewable energy resources (RES) similar to wind, hydro with solar energy micro grid power conditioners as well as active power filters. Mainly of these systems contain a grid linked voltage source converter whose functionality be to synchronize with transfer the variable created power over to the grid. One more feature of the adopted converter is to it be usually pulse width modulated (PWM) by a high switching frequency along with is either current otherwise voltage controlled using a chosen linear or else nonlinear control algorithm. The deciding criterion while selecting the appropriate control scheme generally involves an optimal tradeoff between cost complexity with waveform value needed for meeting latest power quality. The Requirements or else include high parametric sensitivity (now and again both). On the other hand, easy linear proportional integral (PI) controller is level to identified drawbacks as well as the existence of steady state error in the inactive frame along with the must to decouple phase dependence in three phase systems while they are relatively easy to implement. Exploring the simplicity of PI controllers also to improve their overall performance several variation have be proposed in the literature include the adding of a grid voltage feed forward path multiple state feedbacks with increase the proportional gain. Commonly, these variations are able to expand the PI controller bandwidth but unluckily, they as well push the systems towards their constancy limits. An additional disadvantage related by the customized PI controllers is the chance of distort the line current cause by background harmonics introduced along the feed forward path if the grid voltage is unclear. This distortion is able to in turn trigger LC resonance especially when a LCL filter is use at the converter AC output for filtering switching current ripple.

4. PROPORTIONAL CONTROLLER

otherwise, for three-phase systems synchronous casing PI control with voltage feed forward be able to be used but it usually require multiple frame transformations also be able to be complicated to apply using a small cost fixed point digital signal processor (DSP). Overcome the computational burden along with still achieving virtually related frequency reply characteristics as a synchronous frame PI controller develop the Proportional resonant (PR) controller for suggestion track in the stationary frame.

entertainingly the similar control structure be able to use for the precise control of a single phase converter .In the essential functionality of the PR controller is to establish an endless gain at a chosen resonant frequency for eliminate steady state error at that frequency as well as is therefore conceptually related to an integrator whose unlimited DC gain forces the DC steady state error to zero. The resonant portion of the PR controller can so be viewed as a generalized AC integrator (GI) as proven in by the introduce flexibility of change the resonant frequency attempt at using multiple PR controllers for selectively compensate low order harmonics have as well be report in used for three phase active power filters in for three phase uninterruptible power supplies (UPS) with in for single phase photovoltaic (PV) inverters. Base on parallel concept various harmonic reference generators using PR filters have also be proposed for single-phase traction power conditioners.

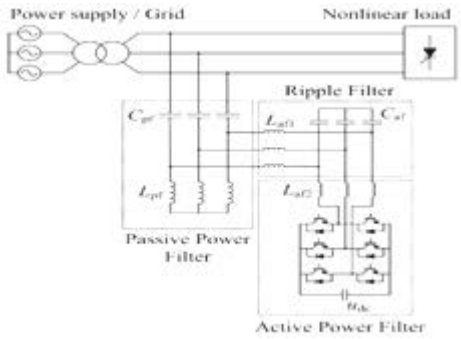


Fig 3 Shunt connected HAPF

converters will locate increasing grid-interfaced applications also as inverters processing DC energy from RES for grid injection or else as rectifiers condition grid energy for dissimilar load usages, this project aims to offer a comprehensive suggestion for reader on the integration of PR controllers with filters to grid connected. The topology is composed of a single tuned branch the control structure as well has to ensure sufficient filter of the current harmonics at other harmonic frequencies. so, designing the controller is an important along with challenging task due to its impact on the performance with stability of the overall system. The control principles previously presented for different HAPF structures are mainly wide band where the proportional (P) control law is the most common and is usually implemented in the SRF . Due to the high value of the proportional constant required for sufficient filtering, the proportional control structure does not perform well with the topology investigated herein. Namely, it shows poor transient performance.

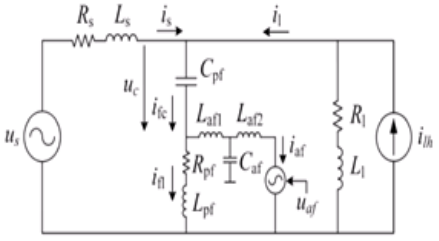


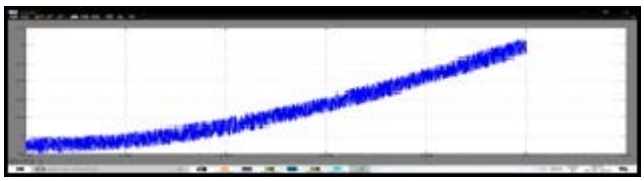
Fig 4 Simplified equivalent circuit of the HAPF

The poor dynamic behavior of this topology in the case of a fluctuating load has also been reported in controllers, where a proportional integral (PI) regulator implemented in the HRF was used to control the active part of the HAPF. To enhance the transient performance of the HAPF, it proposes a proportional resonant current controller implemented in the SRF. Resonant controllers have taken on significant importance in recent years due to their high selectivity and good performance. They are equivalent to the conventional PI controllers implemented in the HRF for the positive and negative sequence reference frames.

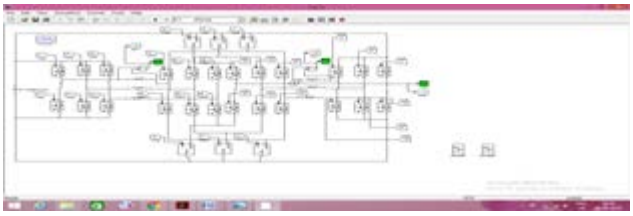
5. SIMULATION RESULTS

Dynamic performance of the presented induction machine, including starting, loading and load changing, are investigated through simulation. The simulated and measured results including speed, capacitor voltage and currents in the rotor and the stator are shown in Figs. 4.2, respectively. The reference speed signals is set to 1400 r/min by controlling the fundamental frequency of IGBTs at 3.3 Hz from t = 0 s. A similar starting procedure is applied both in the simulation.

Fig. 7a: Vtotal i(current wave form)



7b model. Getting error.



Model 8a: Fig: 8a Vtotal

Fig: 8a Vtotal1:

Fig: 8a Vtotal2:

Fig: 8a Vtotal3:

Fig: 8a Vtotal4:

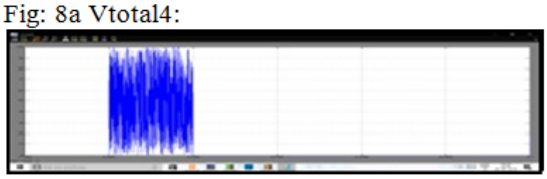


Fig: 8b Model block diagram (subsystem)

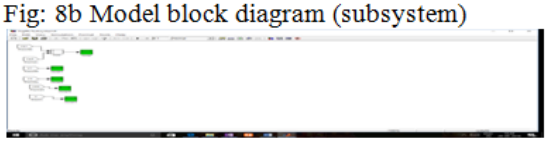


Fig: 8b Vtotal1:

Fig: 8b Vtotal2:

Fig: 8b Vtotal3:

Fig: 8b Vtotal4

Fig: 8b Vtotal

6. CONCLUSION

A multilevel inverter topology has been presented for a four-pole induction-motor drive. The disconnected two IVPWCs are fed from four two-level inverters. All these four two-level inverters are connected to a single dc source minimizing the power balancing issues. The magnitude of dc source voltage requirement is also very less compared with that of conventional five-level inverter topologies. This topology uses only two-level inverters; hence, it is free from capacitor voltage balancing issues. The proposed topology is experimentally verified with a 5-hp four-pole induction motor using a laboratory prototype. Gating pulses are generated using the SPWM technique for the linear modulation region and for the over modulation region using the modified SPWM technique. In the case of any switch failure of the middle two inverters, the topology can be operated as a three-level inverter up to the modulation index of 0.5. This will increase the reliability of the system during fault condition when compared with conventional NPC or FC topologies. This topology does not require any major design modifications of the induction motor except the disconnection of IVPWCs. This concept can also be applied to obtain a higher number of voltage levels for the induction motor with a higher number of poles, which requires more two-level inverters.

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