AREA-DELAY-POWER EFFICIENT 32*32 VEDIC MULTIPLIER USING HAN-CARLSON ADDER

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Abstract—*The goal of this venture is to make proficient use of 32*32 bit Vedic Multiplier. Multiplication process plays a substantial role in digital numeric calculation. Vedic mathematics is the antique method of Indian mathematics which has a distinctive technique of calculations based on 16 sutras (Formulae). In this Vedic mathematics Urdhva Triyakabhyam (UT) multiplication method has been used, which fluctuates from general multiplication process. Vedic multiplier is Longley used in incrementing and decrementing the speed and area respectively. In the anticipated technique area, delay is compared. Here, Han-Carlson adder is by means of to reduce area and delay. The procedures coded in Verilog HDL language by using Modelsim and then comparison is supported in Xilinx ISE 8.1 software.*

Keywords—Multiplier; Han-carlson;Vedic Mathematics; UT; VerilogHDL; Ripplecarry Adder

1. INTRODUCTION

Multipliers play an imperative part in today's digital signal processing and various other applications. with advances in technology many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of outline and hence less area or even mixture of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation.

The communal multiplication process is "add and shift" algorithm. In parallel multipliers number of partial product to be added is the main factors that determine the performance of the multiplier. However with increasing parallelism, the amount of shifts between the partial products and intermediate sums to be added will increase which may result in reduced speed, increase in silicon area due to abnormality of structure and also increased power consumption due to increase in interconnect resulting from complex routing. Instead of "Parallel-Serial "to multipliers compromise speed to achieve better performance for area and power consumption. The selection of a parallel or serial multiplier actually depends on the nature of application. In this lecture we introduce the multiplication algorithms and architecture and compare them in terms of speed, area, power and combination of these metrics.

2. VEDIC MULTIPLIER

Vedic Mathematics is the title given to the olden system of Indian Mathematics which was revived from the Vedas between 1911 and 1918 by Sri Bharati Krishna Tirthaji. According to his research all of mathematics is based on sixteen Sutras, or word-formulae. Perhaps the most arresting feature of the Vedic system is its coherence. This unifying quality is very satisfying; it makes mathematics easy and enjoyable and encourage innovation. In the Vedic system 'difficult' problems or huge sums can often be solved immediately by the Vedic method.

The simplicity of Vedic Mathematics means that calculations can be carried out mentally. There are many advantages in using a flexible, mental system. This leads to more creative, interested and intelligent pupils. Research is being carried out in many areas including the effects of learning Vedic Math on children, developing new, powerful but easy application of the Vedic Sutras in Geometry, Calculus, and Computing. But the real beauty and effectiveness of Vedic Mathematics cannot be fully appreciated without actually practicing the system. One can then see that it is perhaps the most refined and efficient mathematical system possible. It helps a person to solve problems 10-15 times faster. It reduces burden. It provides one line answer. It is a magical tool to reduce scratch work and finger counting.

A. URDHVA-TRIYAKABHYAM

The term Urdhva Triyakabhyam is derived from the Sanskrit language. Urdhva means vertical and Tiryabhyam is crosswise. Urdhva - Triyakabhyam is the general formula applicable to all cases of multiplication and also in the division of a large numbers. It means "vertically and crosswise". This formula is one of the best known of Vedic sutras (formulas), and has found many applications. In fact, as I mentioned in my first post on this topic, there is a whole book dedicated to this sutra. In the below example there are five process to calculate Urdhva Triyakabhyam. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of this partial product

.dissipation of power which outcome in developed expedient act temperature. Therefore it is delay, area and power efficient.

EXAMPLE

STEP 1:

1 4 2

5 3 6

12 ⟶Write 2, 1 carry-over

STEP 2:

1 4 2

5 3 6

1 + 24 + 6 = 31 ⟶ Write 1, 3 carry-overs

STEP 3:

1 4 2

5 3 6

3 + 6 + 10 + 12 = 31 ⟶ Write 1, 3 carry-overs

STEP 4:

1 4 2

5 3 6

3 + 3 + 20 = 26 ⟶ Write 6, 2 carry-overs

STEP 5:

1 4 2

5 3 6

2 + 5 = 7 ⟶Write 7

SOLUTION: 76,112

3. EXISTING METHOD

In existing system 32*32 bit Vedic multiplier is implemented by using four 8*8 multiplier. It is carried out by Kogge stone and ripple carry adder.

A. Ripple Carry Adder

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs as Cin, which is the Cout of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that Cin=0).The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic. In a32-bit ripple-carry adder, there are 32 full adders. So the critical path (worst case) delay is 2(from input to carry in first adder) + 31*31 (for carry propagation in later adders) =95 gate delays.

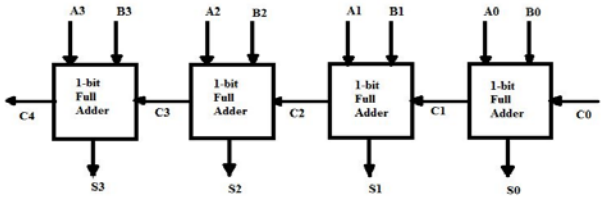

Fig.1.1 Block Diagram of Ripple Carry Adder

B. *Kogge Stone Adder*

KSA is a parallel prefix form of Carry-Ahead adder. It generate carry signal in zero time. It occupies large silicon area. Minimum fan-out at each node. The KSA Increase performance for typical CMOS process nodes and also has low depth. It is used in industries to perform higher arithmetic calculations.

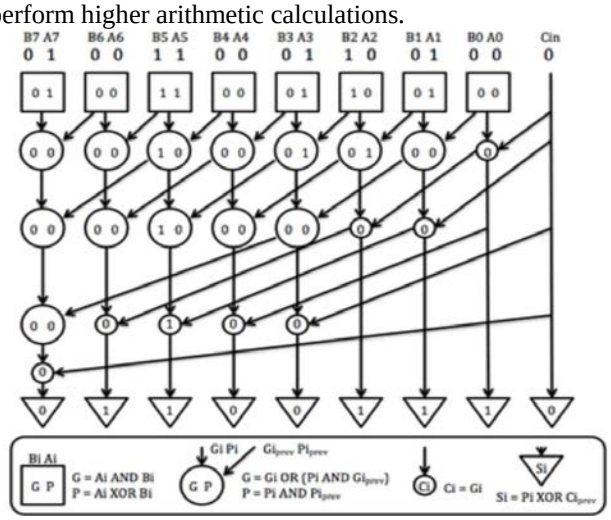

Fig.2.1 Block Diagram of Kogge Stone Adder.

C. Diagram Of Existing Method

In this 32*32 bit Vedic multiplier is intended by means of the on top of 16×16 bit multipliers modules and Kogge Stone Adders(KSA) as shown in the below fig-3.

While for higher order bit addition, the ripple carry adder consumes additional power and more area on the chip and the delay is more, it is better to use at this point the Kogge Stone Adder (KSA) which is proficient adder for higher order addition. The first kogge stone adder adds the outputs of second and third multipliers with the first two higher bytes of the first multiplier. The second adder performs the addition of the output of fourth multiplier and the higher bytes of the first adder. Disadvantage of using kogge stone adder is coverage area is high and increased in delay.

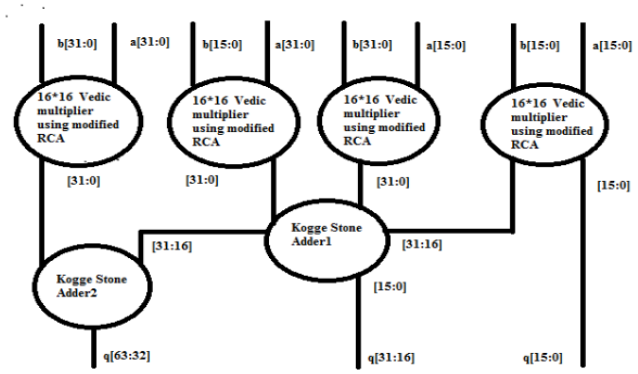

Fig.3.1 Block Diagram of existing 32*32 bit vedic multiplier

4. PROPOSED METHOD

In the proposed method 32*32 bit vedic multiplier is implemented by using han-carlson adder .Han-carlson also proposed a scheme to reduce the complexity of prefix tree.different from kogge stone scheme, this scheme perform carry merge operation on even bits only.generate and propagate signal of odd bits transmitted down the prefix tree.

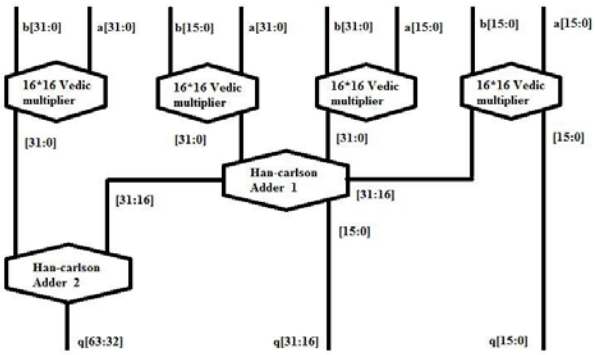

Fig.4.1 Block Diagram of proposed method using Han-Carlson

In the block diagram of Han-Carlson adder there are four 16*16 bit Vedic Multipliers are used. The second and third blocks carry outs the multiplication process and their results are added using the First Kogge stone adder. Now 32 bit output is obtained, the last multiplier block has to be added with the obtained result .But it contains only about 16 bit hence MSB should be added with zeros. And these results should be added with the result of first Kogge stone using the second kogge stone adder. And this result should be added with the first 16*16 Vedic multiplier using the last kogge stone adder.

When we compare with Kogge stone adder, the Area, Delay and Power can be reduced in Han-Carlson adder.

5. RESULT

This section reveals the simulation results, delay and area comparison of 16×16 bit Vedic multipliers and proposed 32×32 bit Vedic multiplier. The simulation results for 16×16 bit Vedic multipliers. It shows the output for maximum value of inputs,

a =11111100000010101010101101010111

b =11110000111111110000111110011001

c=0

Then the output becomes

s=11101111111100111111000011110011

c=1

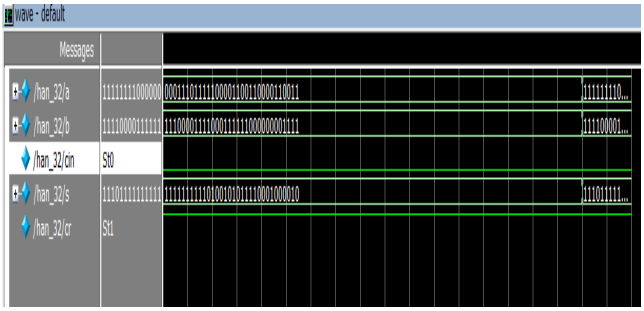

Fig.5.1 Simulation result of 32*32 bit Vedic multiplier

The table I illustrates that the area, delay and power comparison of 32*32 bit Vedic multipliers in three levels of logic in each multiplier. When the design is formed by using kogge stone adder the delay is 53.1370ns.By replace kogge stone adder with Han-Carlson adder the delay is reduced as 43.928ns.From the table we can conclude that the area coverage using kogge stone adder is 15,682 and reduced into 15,532 by han-carlson. There is also reduction in power as 419mW using Han-Carlson adder from 420mW.

Multiplier Existing multiplier using KSA
Proposed multiplier using Han-Carlson

DELAY (ns)
53.13
43.92

AREA
15,682
15,532

POWER(mW)

420
419

TABLE-I COMPARISON RESULT OF 32*32 BIT VEDIC MULTIPLIER

Multiplier	Existing multiplier using KSA	Proposed multiplier using Han-Carlson
DELAY (ns)	53.13	43.92
AREA	15,682	15,532
POWER(mW)	420	419

6. CONCLUSION

Multiplication process is the one of the most vital arithmetic operation. Instead of using normal multiplication process we used Vedic multiplier to make complex calculation into simpler one. The simulation shown using kogge stone adder for the parameters like delay, area and power had consumption is more. But when we use Han-Carlson adder the consumption of delay, area and power is reduced. The above tabulation exposed that comparison among kogge stone adder and Han-Carlson. This has been proved that Han-Carlson consumes less area delay and power.

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