ANALYSIS OF A NEW THREE PHASE MULTILEVEL INVERTER WITH SHARED POWER SWITCHES

Maheswari K T[1] | P.Nandhini Devi[2] | M.Swathy[3] | Sudhapriya[4]
[1](Asst prof, Dept of EEE, Bannari Amman Institute of Tech, Sathyamangalam, maheswarikt@bitsathy.ac.in)
[2](Dept of EEE, UG Scholar, Bannari Amman Institute of Tech, Sathyamangalam, nandhuperiyasamy@gmail.com)
[3](Dept of EEE, UG Scholar, Bannari Amman Institute of Tech, Sathyamangalam, swathysivagami@gmail.com)
[4](Dept of EEE, PG Scholar, Bannari Amman Institute of Tech, Sathyamangalam)

Abstract—*This paper suggests a new 3-phase multilevel inverter that is able to generate 7 levels in line-to-line voltage by only 11 switches. The inverter is designed from the 6 -switch conventional full- bridge topology with the adding of 5 bidirectional switches in which 2 of them are shared between the three phases. By performance so, the number of power switches can be minimized, so reducing the complexity in generating and controlling PWM signals. The performance of the inverter and the effectiveness of the modulation technique are verified using MATLAB/SIMULINK.*

Keywords—Multilevel inverter, Power switches, PWM signal

1. INTRODUCTION

The obvious drawbacks of conventional 2-level, full-bridge inverters have paved the way for multilevel inverters. Multilevel inverters are able to produce near-sinusoidal voltage waveforms that can provide high voltage capability and reduced harmonic content. In overall, multilevel inverters can be categorized into 3 major types: the diode-clamped type, the capacitor-clamped type, and the cascaded H-bridge cells type. The development of advanced topologies have flourished of late in response to several issues related to circuit complexity, total cost, efficiency, and output quality. The asymmetric cascaded H-bridge multilevel inverter is an example of those topologies. It is built by supplying imbalanced DC voltage amplitudes at each stage of the H-bridge cells. In a mixed-level topology the normal H-bridge cell in a cascaded multilevel inverter is basically replaced by other cell types such as the diode-clamped-type cell. In another topology, known as multistage topology, there are at least 2 stages in a cascaded multilevel inverter that are of dissimilar configurations, such as by joining the 3-phase 2- levelfull-bridge inverter as the main stage, with H-bridge cells at each arm as the secondary stage. To control these inverters, both high and low switching frequency approaches have been applied.

Multilevel inverters (MLIs) can be used to solve these problems. They are built using a number of cells; each cell consisting of switches and capacitor voltage sources. The control of the power switches allows the capacitor voltage sources to be added to obtain the desired output voltage with reduced voltage stress on each individual switch. Also, the resolution of the staircase waveform of the output voltage increases with the number of voltage steps of capacitor voltage sources For instance, multicarrier PWM strategy, space vector modulation, and carrier-based space vector modulation fall under high switching frequency approaches, while voltage vector approximation and selected harmonic elimination are examples of low switching frequency methods.

2. THE PROPOSED TOPOLOGY

Figure 1 shows the proposed circuit topology consisting of an auxiliary circuit created from 5 bidirectional switches and a 6- switch full-bridge configuration. The line-to-line output voltage waveform is formed from 7 levels of the following amplitudes: {-3Vdc ,-2Vdc , -Vdc , Vdc, 2Vdc, 3Vdc, and 0}. For operation at the fundamental frequency in order to obtain stepped waveforms in the line-to-line output voltages, 18 operational modes are defined within a period in order to achieve 3-phase voltages at the load. Table 1 presents the description of the 18 modes and the status of their corresponding switches.

From Table 1 it can be detected that if the output voltages operate at fundamental frequency f , then QA1 , QA2 , QB1 , QB2 , QC1 , and QC2 also operate at the same frequency f ; QA3 , QB3 , and QC3 operate at frequency 2f , and QX and QY operate at frequency 3f . It can

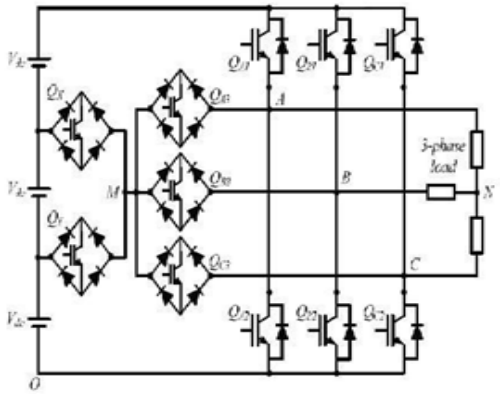

Fig: 1 The proposed multilevel inverter circuit topology

also be seen that QA1, QA2, and QA3 are exclusively used for phase A; QB1 , QB2 , and QB3 are utilized for phase B; and QC1 , QC2 , and QC3 are utilized for phase C. However, in the case of QX and QY, both are shared among the three phases. This unique feature offered by the proposed topology further helps in reducing the number of switches used, thus greatly simplifying the circuit complexity. In fact, the proposed topology offers the minimum number of switches, namely 11 switches, as compared with the 3 well-known topologies that generate the same number of output voltage levels with 18 switches a record of 38.89% less in terms of the total number of switches employed. The figure 1 shows the proposed multilevel inverter circuit topology of the project

3. CIRCUIT DIAGRAM EXPLANATION

The proposed circuit topology consisting of an auxiliary circuit constructed from 5 bidirectional switches and a 6-switch full-bridge configuration. The line-to-line output voltage waveform is formed from 7levels of the following amplitudes: -3Vdc, -2Vd, -Vdc, Vdc, 2Vdc, 3Vdc, and 0.
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4. SWITCHING SEQUENCE

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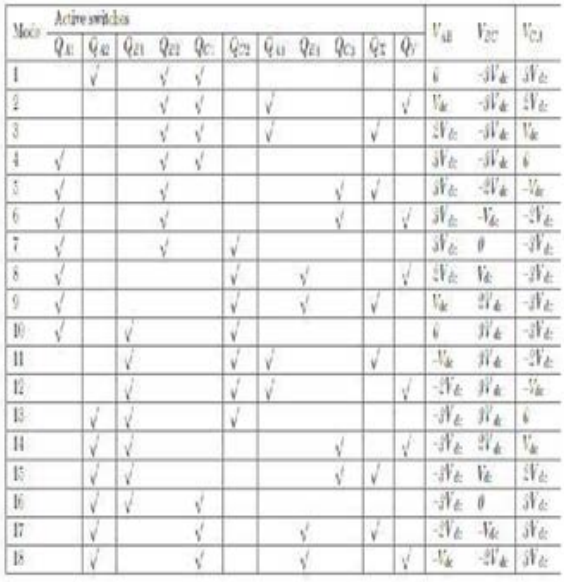
TABLE 1: SWITCHING SEQUENCE OF THE PROPOSED INVERTER



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Switching states (S_J)	Status of switch					V_{JO}
	Q_{J1}	Q_{J2}	Q_{J3}	Q_X	Q_Y	
0	Off	**On**	Off	Off	Off	0
1	Off	Off	**On**	Off	**On**	V_{dc}
2	Off	Off	**On**	**On**	Off	$2V_{dc}$
3	**On**	Off	Off	Off	**Off**	$3V_{dc}$

J – A, B, C.

Table 2: Definition of switching states Table 2 describes the definition of switching states. State 0 results in VJO = 0 and State 1 leads to VJO = Vdc, while State 2 and State 3 refer to VJO = 2Vdc and VJO = 3Vdc, respectively, where J is the phase identity. 35Considering only one phase, say phase A, State 0 is achieved when onlyQA2 is turned on, State 1 appears when QA3 and QY are active, and State 2 is obtained when QX replaces QY as the active switch together with QA3 .

5. RESULTS AND DISCUSSION

THREE PHASE 11 SWITCH MULTILEVEL INVERTER

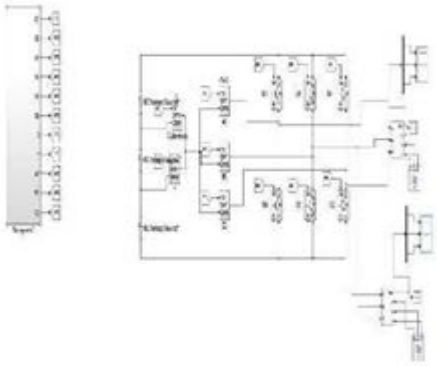

Fig: 2 11 Switch Three Phase Multilevel Inverter

Thus the Fig 2 shows the Matlab/Simulink circuit of 11 Switch Three Phase Multilevel Inverter.
The activation of QA1 alone results in State 3. The same goes for phases B and C, too. With respect to the three arms, 46 possible switching state combinations can be created in the form of SA SB SC in which SA denotes the switching state of phase A, SB for phase B, and SC for phase C.

A. OUTPUT FOR THREE PHASES 11 SWITCH MULTILEVEL INVERTER:

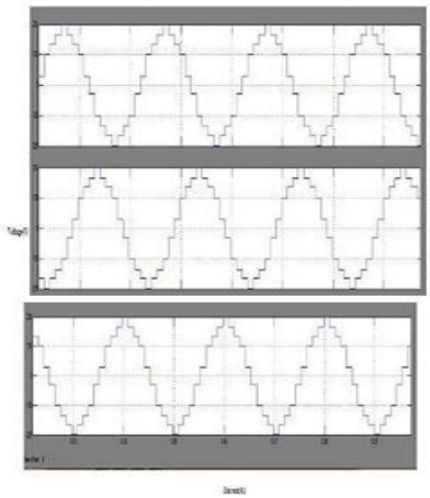

Fig: 3 Phase voltage of 11 Switch Three PhaseMultilevel Inverter

Fig: 4 Line voltage of 11 Switch Three Phase Multilevel Inverter.Thus the Fig 3 and 4 shows the Phase and Line voltages of 11 Switch Three Phase Multilevel Inverter.

B. THREE PHASE 11 SWITCH MULTILEVEL INVERTER USING PWM

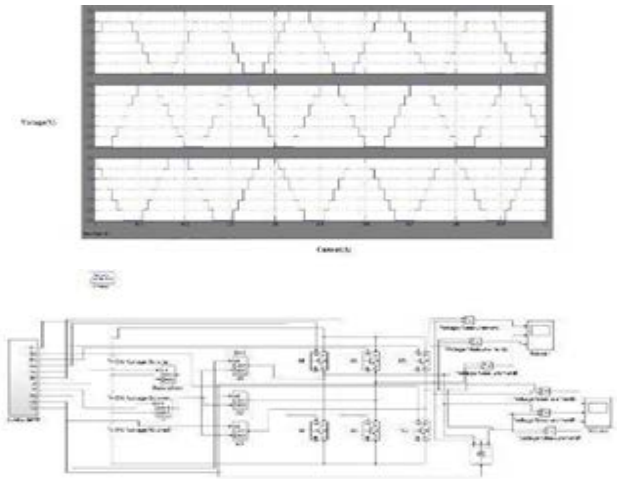

Fig: 5 11 Switch Three Phase Multilevel Inverter using PWM

Thus the Fig 5 shows the Matlab/Simulink circuit of 11 Switch Three Phase Multilevel Inverter using PWM.

6. MATLAB/SIMULINK OUTPUT FOR THREE PHASE 11 SWITCH MULTILEVEL INVERTER

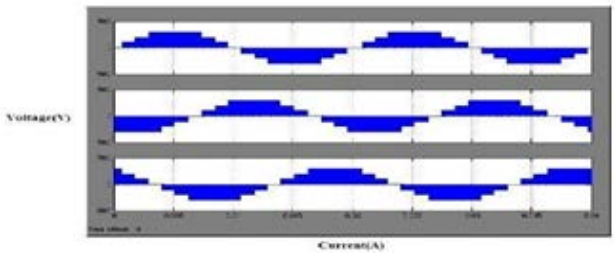

Fig: 6 Phase voltage of 11 Switch Three Phase Multilevel Inverter using PWM

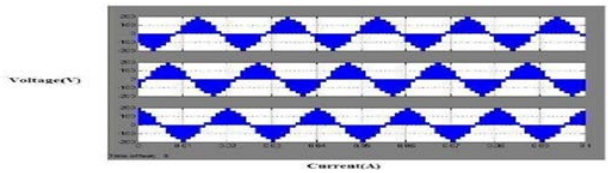

Fig: 7 Line voltage of 11 Switch Three Phase Multilevel Inverter using PWM

Thus the Fig 6 and 7 shows the Phase and Line voltages of 11 Switch Three Phase Multilevel Inverter using PWM.

7. CONCLUSION

In this paper, a new multilevel inverter generating 7-level line-to-line output voltages that uses the minimum number of power switches (only 11 switches as opposed to other equivalent topologies) has been presented. The significant reduction in the number of switches is achieved by sharing two bidirectional switches (QX and QY) among the three phases, thus greatly reducing complexity. Although the number of diodes employed increases through the use of bidirectional switches, the fact that diodes are much cheaper than power switches such as IGBTs contributes to a reduction in the overall cost. Thus the MATLAB/SIMULINK model for the circuit is simulated and the results were verified.

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